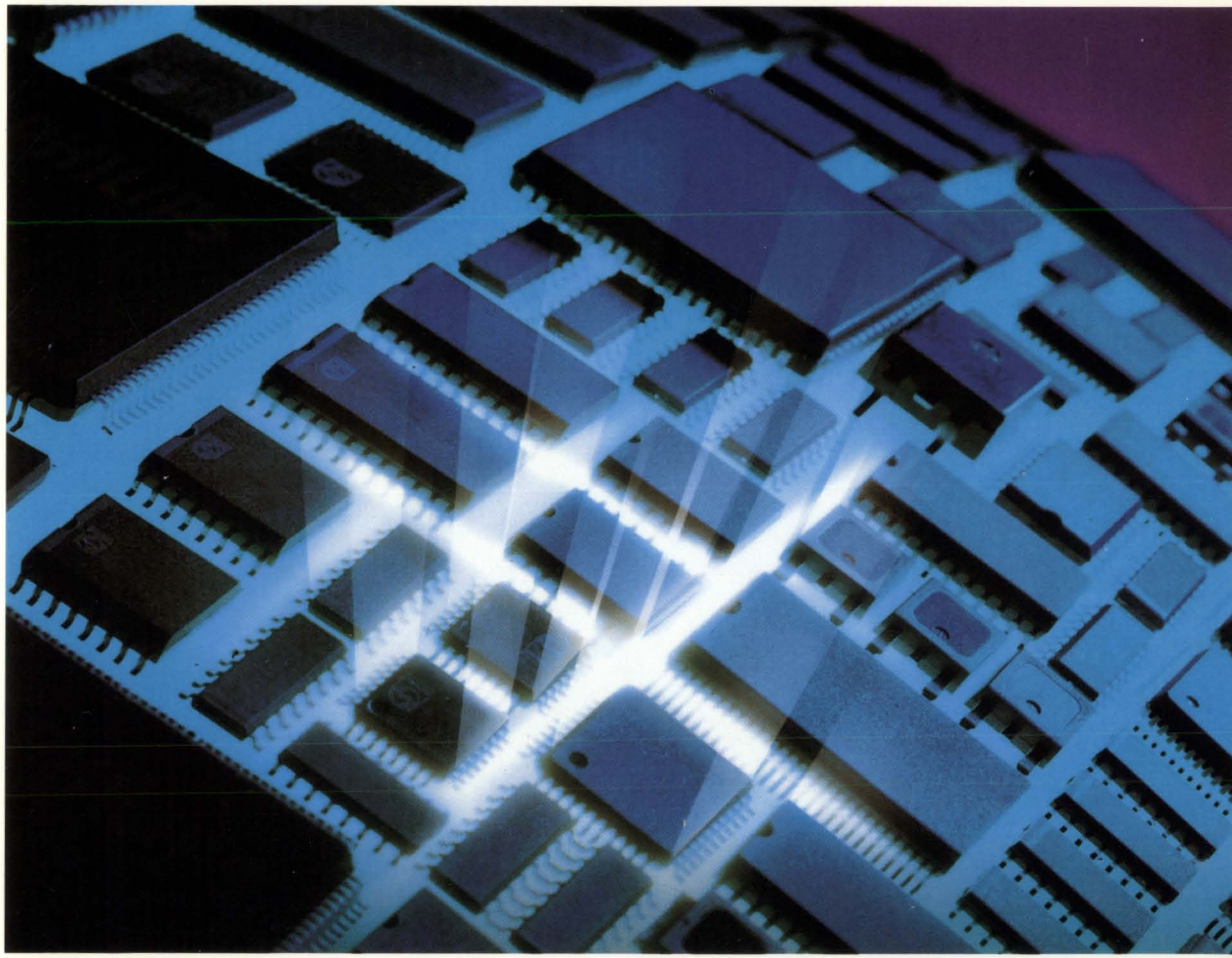
INTEGRATED CIRCUITS

Advanced Low-power Schottky Logic



1997

Data Handbook IC05

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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Advanced Low-power Schottky (ALS) Logic

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PRODUCT STATUS

DEFINITIONS		
DATA SHEET IDENTIFICATION	**PRODUCT STATUS**	**DEFINITION**
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Section 1
General Information

Advanced Low-power Schottky Logic (ALS)

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ADVANCED LOW-POWER SCHOTTKY LOGIC

CONTENTS

Introduction

FEATURES

- 4ns propagation delays
- 1.2 mW/gate power dissipation
- Guaranteed AC performance over temperature and extended V_{CC} range: 5V ± 10%
- High impedance PNP base input structure for reduced bus loading in low state
- Standard TTL functions and pinouts
- Replacement for LS types are 1/2 the power and twice the speed
- 2kV ESD protection

PRODUCT DESCRIPTION

Philips Semiconductors has combined advanced oxide isolated fabrication techniques with standard TTL functions to create its ALS product line. Low input loading allows the user to mix LS, FAST and HCMOS in the same system without the need for translators and restrictive fanout requirements.

ALS circuits are pin–for–pin replacements for LS types, but offer dissipation 2 to 3 times lower, and higher operating speeds. Existing systems can achieve much lower power and improved performance by replacing the LS types with the corresponding ALS devices.

The input structure provides better noise immunity due to higher thresholds, while the oxide–isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Philips Semiconductors guarantees all AC parameters under realistic system conditions — across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

Clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pull up resistors.

Multiple sources and a family of powerful circuits make Philips Semiconductors ALS a wise TTL choice.

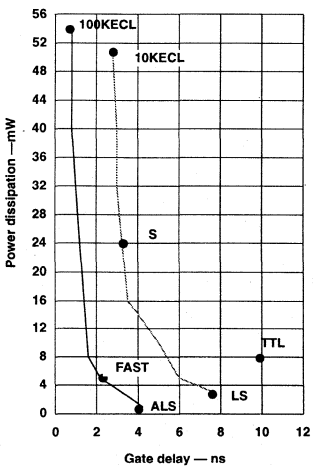


Figure 1. The speed/power spectrum

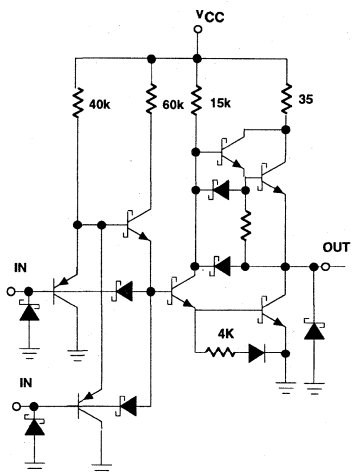


Figure 2. Basic ALS gate

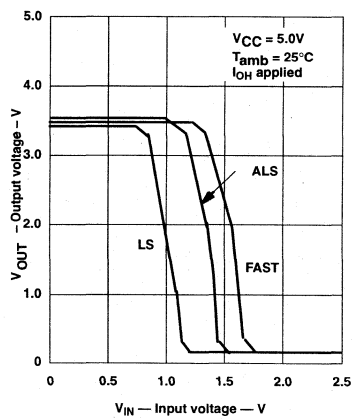


Figure 3. Transfer functions at room temperature

Introduction

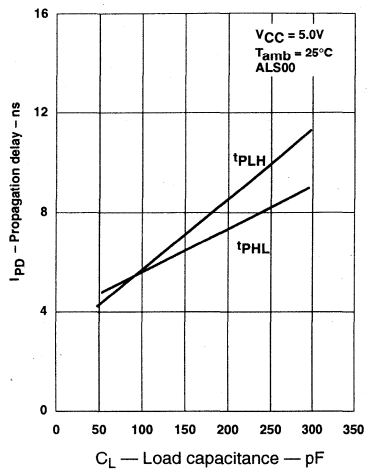


Figure 4. Propagation delay vs load capacitance

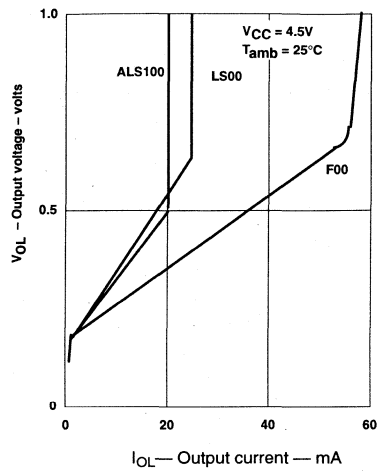


Figure 5. Output low characteristics

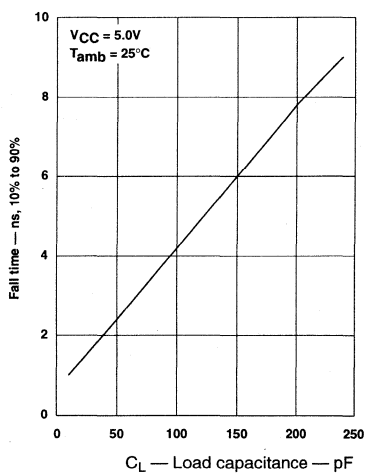


Figure 6. Fall time vs load capacitance

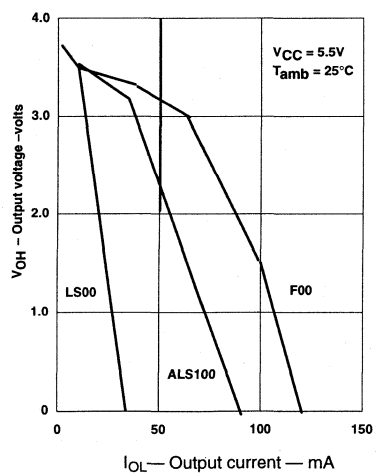


Figure 7. Output high characteristics

Functional selection guide

GATES

FUNCTION		DEVICE NUMBER	NUMBER OF PINS
INVERTERS	Hex inverters	74ALS04B	14
NAND	Quad 2–input	74ALS00A	14
	Triple 3–input	74ALS10A	14
	Dual 4–input	74ALS20A	14
	8–input	74ALS30A	14
	Quint 2–input NAND, open collector	74ALS38A	14
NOR	Quad 2–input	74ALS02	14
	Triple 3–input	74ALS27	14
AND	Quad 2–input	74ALS08	14
	Triple 3–input	74ALS11A	14
OR	Quad 2–input	74ALS32	14
Exclusive OR	Quad 2–input	74ALS86	14

FLIP–FLOPS

FUNCTION	DEVICE NUMBER	NUMBER OF PINS	CLOCK EDGE	INV	NINV
D	74ALS74A	14	↑	X	X
JK	74ALS109A	16	↑	X	X
JK	74ALS112A	16	↓	X	X
Quad D	74ALS175	16	↑	X	X
Hex D	74ALS174	16	↑		X
Octal D	74ALS273	20	↑		X
Octal D with enable	74ALS377	20	↑		X
Octal D, 3–State	74ALS374	20	↑		X
Octal D, 3–State	74ALS564A	20	↑	X	
Octal D, 3–State	74ALS574A	20	↑		X

LATCHES

FUNCTION	DEVICE NUMBER	NUMBER OF PINS	INV	NINV	3–STATE
Octal	74ALS373	20		X	X
8–bit transparent	74ALS563A	20	X		X
8–bit transparent	74ALS573A	20		X	X

MULTIPLEXERS/ENCODERS

FUNCTION	DEVICE NUMBER	NUMBER OF PINS	INV	NINV	3–STATE
Dual 4–input	74ALS153	16		X	
Dual 4–input	74ALS253	16		X	
Quad 2–input	74ALS157	14		X	
Quad 2–input	74ALS158	14	X	X	
Quad 2–input	74ALS257	16		X	X
Quad 2–input	74ALS258	16	X		X
8–bit	74ALS151	16	X	X	
8–bit	74ALS251	16	X	X	X

Functional selection guide

DECODERS/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	NUMBER OF PINS
Dual 1–of–4	74ALS139	16
1–of–8	74ALS138	16

BUFFERS

FUNCTION	DEVICE NUMBER	NUMBER OF PINS	INV	NINV	3–STATE
Octal buffer	74ALS240A/240A–1	20	X		X
Octal buffer	74ALS241A/241A–1	20		X	X
Octal buffer	74ALS244A/244A–1	20		X	X

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	NUMBER OF PINS	BIT	CLOCK EDGE	SERIAL IN	PARALLEL IN	SERIAL OUT	PARALLEL OUT
Shift register	74ALS164	14	8	↑	X			X

COUNTERS

FUNCTION	DEVICE NUMBER	NUMBER OF PINS	TYPE	PRESETTABLE	PARALLEL ENTRY	CLOCK EDGE
Synchronous	74ALS161B	16	BCD	X	Synchronous	↑
Synchronous	74ALS163B	16	BCD	X	Synchronous	↑

TRANSCEIVERS

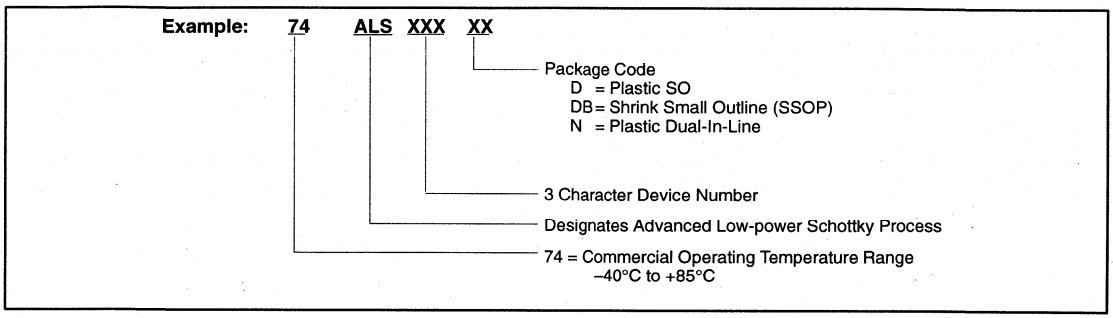
FUNCTION	DEVICE NUMBER	NUMBER OF PINS	INV	NINV	3–STATE
Octal transceiver	74ALS245A/245A–1	20		X	X
Octal transceiver	74ALS645A/645A–1	20		X	X
Octal transceiver	74ALS620A/620A–1	20	X		X
Octal transceiver	74ALS623A/623A–1	20		X	X
Octal latched transceiver	74ALS543/543–1	24		X	X
Octal latched transceiver	74ALS544/544–1	24	X		X
Octal transceiver/register	74ALS646/646–1	24		X	X
Octal transceiver/register	74ALS648/648–1	24	X		X
Octal transceiver/register	74ALS651/651–1	24	X		X
Octal transceiver/register	74ALS652/652–1	24		X	X

Ordering Information

Philips Semiconductors ALS products are generally available in both standard dual-in-line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial products, the standard temperature range is 0° – 70° C. Available options are shown on individual data sheets in the Ordering Information table. For surface mounted devices, the SO plastic dual-in-line package is supplied up to and including 24 pins.

Ordering code example

ALS PRODUCTS



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
Commercial range T_{amb} = 0°C to +70°C	74ALSXXX	N = Plastic Dual In–Line D = Plastic SO or SOL Dual In–Line DB= Plastic SSOP Type II

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

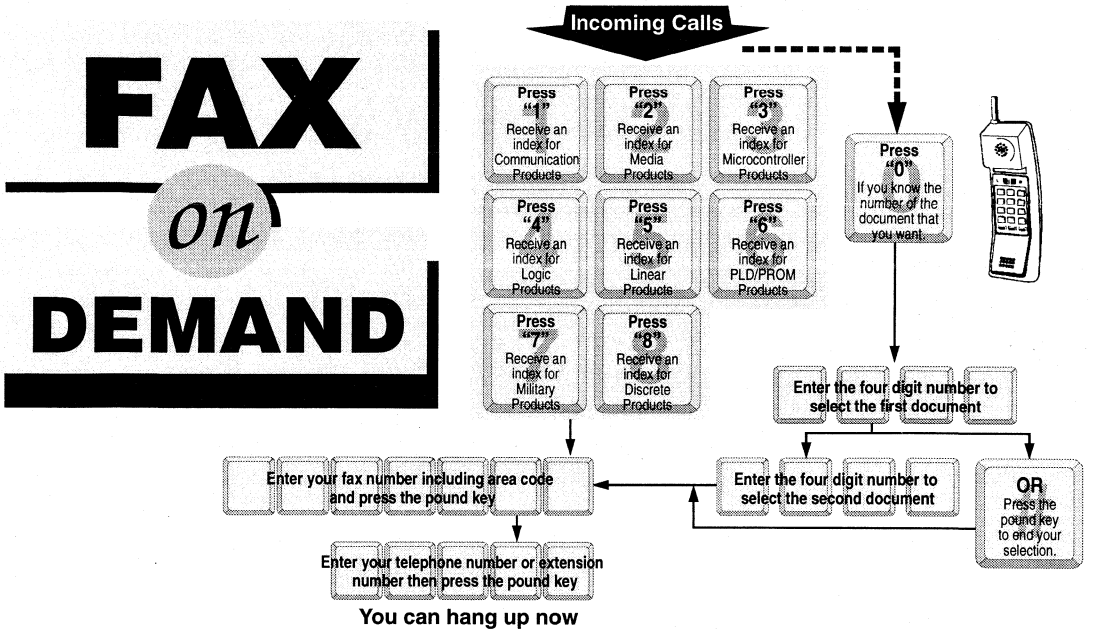
CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

FAX-on-DEMAND System



What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
http://www.semiconductors.philips.com

Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

FAX-on-DEMAND phone numbers:

England (United Kingdom, Ireland)	44-181-730-5020
France	33-1-40-99-60-60
Germany (Austria, Switzerland)	49-40-23536-357
Italy	39-167-295502
North America	1-800-282-200

Locations soon to be in operation:

Hong Kong
Japan
The Netherlands

Internet World Wide Web Home Page

WHAT IS IT?

Welcome to our place in cyberspace. The Logic Products Group now has its own home page within Philips Semiconductors. Explore our Web pages and travel the road that offers the smoothest path from 5 volts to 3 volts. In addition, we offer you the latest information on Products, News, Support, Employment and Offices.

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For access to the Philips Semiconductors Home Page go to the World Wide Web location:

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You can find us in the Product category of *Digital Products*.

Design considerations

INTRODUCTION

The properties of ALS logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing ALS systems, but a reference for some of the constraints and techniques to be considered when designing a high speed system.

HANDLING PRECAUTIONS

As described in the circuit characteristics, ALS devices are susceptible to damage from electrostatic discharge (ESD).

- Philips Semiconductors ALS devices are shipped in conducting foam or anti–static tubes and foil–lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of ALS devices, make sure that the individual is grounded and all handling means (such as tools, fixtures, and benches) are grounded.
- After removal from the shipping material, the leads of the ALS devices should always be grounded. In other words, ALS devices should be placed leads–down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on–off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- ALS inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10k ohm should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static–generating materials.

INPUT CLAMPING

ALS circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long duration, negative pulses.

UNUSED INPUTS

Proper design rules dictate that all unused inputs on TTL devices be tied either high or low. This is especially important with ALS logic.

Electrically open inputs can downgrade AC noise immunity as well as the switching speed of the device. Tying inputs to V_{CC} or ground, directly or through a resistor, protects the device from in–circuit electrostatic damage.

ALS devices do not require an input resistor to tie the input high. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active–high NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active–high NOR or OR inputs to ground.
3. Connect the unused active–high NAND or AND inputs to the output of an unused gate that is forced high.

MIXING ALS WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74ALS is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired power features.

The speed/power characteristics of the ALS devices are achieved partially by the internal rise and fall times, as well and those at the input and output nodes. These transitions can cause noise of various types in a system. Power and ground noise are generated by the transitions of the current in the output load capacitance. Signal line noise can also be generated by the output transitions.

The noise generated by ALS devices can be minimized in systems designed with shorter signal lines, good ground planes, well–by–passed power distribution networks, layouts that minimize adjacent signal lines that run parallel, and improved impedance matching in signal lines to reduce transmission line type reflections.

INPUT LOADING AND DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and output drive characteristics of each family are different and must be taken into consideration when mixing them in a system. Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

INPUT OUTPUT LOADING AND FAN OUT TABLE

For convenience in system design, the input–output loading and fan out characteristics of each circuit are specified in terms of unit loads and actual load value. One ALS Unit Load (U.L.) in the high state is defined as 20μA; thus both the input high leakage current, I_{IH}, and output high current–sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one ALS Unit Load (U.L.) in the low state is defined and 0.1mA, and both the input low current I_{IL}, and the output low current sinking capability, I_{OL}, are normalized to 0.1mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

CLOCK PULSE REQUIREMENTS

All ALS clock inputs are buffered to increase their tolerance of slow positive–clock edges and heavy ground noise. Nevertheless, the rise time on positive–edge–triggered devices should be less than the nominal clock–to–output delay time measured between 0.8V to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean clock pulse is required, but the path between the clock drive and clock input of the device should be well shielded from electromagnetic noise.

Design considerations

TABLE 1. LOADING COMPARISONS

DRIVING DEVICE FAMILY	I_{OL} (min)	DRIVEN DEVICE FAMILY					
		74F	74F (NPN)	74LS	74	74S	74ALS
		I_{IL} (max)					
		0.6mA	20μA	0.4mA	1.6mA	2.0mA	0.1mA
		Maximum number of loads driven					
74F	20mA	33	1,000	50	12.5	10	200
74F (NPN)	64mA	106	3,200	160	40	32	640
74LS	8mA	13	400	20	5	4	80
74LS buffer	24mA	40	1,200	60	15	12	240
74	16mA	26	800	40	10	8	160
74 buffer	40mA	78	2,400	120	30	24	400
74S	20mA	33	1,000	50	12.5	10	200
74S buffer	60mA	100	3,000	150	37.5	30	600
74ALS	8mA	13	400	20	5	4	80
74ALS buffer	24mA	40	1,200	60	15	12	240
74ALS –1 version	48mA	80	2,400	120	30	24	480

ALS OUTPUTS TIED TOGETHER

The only ALS outputs that are designed to be tied together are open collector and 3–State outputs. Standard outputs should not be tied together unless their logic levels will always be the same; either all high or low. When connecting open collector or 3–State outputs together, some general guidelines must be observed.

OPEN COLLECTOR OUTPUTS

These devices must be used whenever two or more OR–tied outputs will be at opposite logic levels at the same time. These devices must have a pull–up resistor (or resistors) added between the OR–tie connector and V_{CC} to establish an active–high level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull–up resistor is determined as follows:

$$R\ (min) = \frac{V_{CC}\ (max) - V_{OL}}{I_{OL}\ (max) - N_2\ (I_{IL})}$$

$$R\ (max) = \frac{V_{CC}\ (min) - V_{OH}}{N_1\ (I_{OH}) + N_2\ (I_{IH})}$$

where:

I_{OL} = Minimum I_{OL} guarantee or OR–tied element

$N_2\ (I_{IL})$ = Cumulative maximum input low current for all inputs tied to OR–tie connection

$N_1\ (I_{OH})$ = Cumulative maximum output high leakage current for all outputs tied to OR–tie connection

$N_2\ (I_{IH})$ = Cumulative maximum input high leakage current for all inputs tied to OR–tie connection.

If a resistor divider network is used to provide the high level, the R (max) must be decreased enough to provide the required [(V_{OH}/R) (pull down)] current.

3–STATE OUTPUTS

3–State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3–State output should be active at any time. This generally requires that the output enable signals be non–overlapping. When TTL decoders are used to enable 3–State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non–overlapping signals cannot normally guarantee when the address is changing.

Since most 3–state output enable signals are active–low, shift registers or edge–triggered storage registers provide good output enable buffers. Shift registers with one circulating low bit, such as the 'ALS164 is ideal for sequential enable signals. The 'ALS174 or 'ALS273 can be used to buffer enable signals from TTL decoder or microcode (ROM) devices. Since the outputs of these registers will change from low–to–high faster than from high–to–low, the selection of one device at a time is assured.

GROUND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un–bypassed V_{CC} runs from 50 ohm to 100 ohm, depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50 ohm dynamic load and the buffer low–to–high transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

Design considerations

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = \frac{0.4A \times 3 \times 10^{-9}\ sec}{0.1V}$$

$$= 12 \times 10F^{-9}$$

$$= 0.012\mu F$$

The formula is derived as follows:

$$Q = CV$$

By differentiation:

$$\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$$

Select the C bypass ≥ 0.02µF and try to use a high quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to take care of board–level current transients.

CROSS TALK

The best way to handle cross talk is to prevent it from occurring in the first place; quick–fixes are troublesome and costly. To prevent cross talk, maximize spacing between signal lines and minimize spacing between signals and ground lines. Preferably, place ground lines between signal lines. For added precaution, add a ground trace alongside either the potential cross–talker or the cross–listener.

For backplane or wire–wrap, use twisted pair of sensitive functions such as clocks, asynchronous set or reset, or asynchronous parallel load. In flat cable, make every other conductor ground.

For multilayer P. C. boards, run signal lines in adjacent planes perpendicular to prevent coupling, and limit capacitive coupling, Use power shield (V_{CC} or ground plane) in between signal lines.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristics impedance will help reduce cross–talk.

Since $\frac{\Delta Q}{\Delta t} = I$

the equation becomes $I = C\frac{\Delta V}{\Delta t}$

hence, $C = \frac{I\,\Delta V}{\Delta t}$

Data Sheet Specification Guide

INTRODUCTION

Philips Semiconductors ALS data sheets have been configured for quick usability. They are self–contained and should require minimum reference to other sections for further information.

FEATURES AND DESCRIPTION

Features and/or Descriptions are shown starting at the top of the first page of the data sheets for quick reference.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed in the FEATURE of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of V_{CC} = 5.0V and T_{amb} = 25°C.

The typical I_{CC} current shown in that same specification block is the average current (In the case of gates, this will be the average of I_{CCH} and I_{CCL} currents) at V_{CC} = 5.0V and T_{amb} = 25°C. It represents the total current through the package, not the current through the individual functions.

LOGIC SYMBOLS

The logic symbols explicitly shows the internal logic (except for complex logic).

IEC/IEEE SYMBOLS

The IEC/IEEE symbols found in this handbook are in accordance with the IEC and IEEE standards. The logic symbols are described in

IEEE Standard
Graphic Symbols for Logic Functions
ANSI/IEEE Std 91–1984
(Review of ANSI/IEEE Std 91–1973

which can be ordered through
IEEE Service Center IEEE Service center
445 Hoes Lane
Piscataway, New Jersey 08854
Phone: 201–981–0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it. There is no implication that the part will function at these extreme conditions, Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than –0.5V is applied to the output pin, after the voltage is removed, the part will not have been shorted.

Input and output voltage specifications in this table reflect the device breakdown voltage in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (–0.5V).

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to all ALS devices, which should not be exceeded under the worst probable conditions.

These values are chosen by Philips Semiconductors to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The user should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices.

Absolute maximum ratings imply that any transient voltages, currents, and temperatures should not exceed the maximum ratings.

Family Specifications for Absolute Maximum Ratings are shown in Table 1.

TABLE 1. ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	Standard outputs	16	mA
		3–state and buffer outputs	48	mA
		–1 version outputs	96	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions table has a dual purpose. In one sense, it sets some environmental conditions (operating case temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Philips Semiconductors, but as the conditions Philips Semiconductors uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Philips Semiconductors feels strongly that the specifications set forth in a data sheets should reflect as accurately as possible the operation of the part in an actual system.

In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment. If V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by DC electrical characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth–table exercise" mode. This frequently causes problems because of the noise present at the test head for automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done slowly., on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, the V_{IH} and V_{IL} should never be used in testing the functionality of any ALS part type. For these types of tests, input voltages of +4.5V and 0.0v should be used for high and low state respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" highs and lows during functional testing is done typically present at the test heads of automated test equipment especially when using cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Family Specifications for recommended operating conditions are shown in Table 2.

TABLE 2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
V_{OH}	High–level output voltage	Open collector			5.5	V
I_{OH}	High–level output current	Standard			–0.4	mA
		3–State			–2.6	mA
		Buffers			–15	mA
I_{OL}	Low–level output current	Standard			8	mA
		3–State and buffers			24	mA
		–1 version			48[1]	mA
T_{amb}	Operating free air temperature range		0		+70	°C

Note to recommended operating conditions

1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Philips Semiconductors during their testing operations conducted under the conditions set forth in the recommended operating conditions table.

V_{OH} and V_{OL} values vary depending on the V_{CC} values specified and the type of output structure; standard, 3–State, or buffer. Generally, as the output current and V_{CC} variations increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Philips Semiconductors specifies and tests V_{OH} and V_{OL} for 10% V_{CC} swings.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structure being tested. PNP and diode inputs are tested with V_{CC} = MAX and 7.0V at the input. When I_I is measured on transceiver I/O pins, both V_{CC} and the input voltage are 5.5V., The reduced input voltage is necessary because of the output structure connected to the input structure. Output structure breakdown sooner than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both diode and PNP input structures is less than mA typically. I_{IL} is less than 100μA for PNP inputs and less than 200μA for diode inputs. If multiple structures are tied together in the design, then the input current values also multiply.

For transceiver I/O pins the outputs are in high impedance state when the inputs are tested. Therefore, the small amount of extra leakage is combined with the I_{IH} andf I_{IL} specifications.

I_{OZH} is tested with setup conditions that would put the output in the high state if it were not in the 3–State high–impedance

condition, I_{OZL} is similar except the setup condition is for low state.

I_{OH} is tested only on open collector outputs and leakage test for the lower output transistor structure. V_{CC} is less than V_{OH} so that there is not a current path to or from V_{CC} that would mask the leakage.

IO is approximately one half of the true short circuit output current value. It is measured at 1/2 V_{CC} in a linear region of the low state output current characteristics. The method of testing allows indirect measurement of the current available for capacitive load charging while avoiding circuit test problems of over–heating and potential circuit damage associated with I_{OS} tests.

Family speciication for DC electrical characteristics are shown in table 3.

TABLE 3. DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[2]	LIMITS			UNIT	V_{CC}[4]
				MIN	TYP[2]	MAX		
V_{IK}	Input clamp diode voltage		V_{CC} = MIN, I_{IN} = 18mA			-1.5	V	MIN
V_{OH}	High-level output voltage	Standard[5]	I_{OH} = –0.4mA	V_{CC} – 2			V	5V ± 10%
		3-State	I_{OH} = –2.6mA	2.4	3.2		V	MIN
		3-State	I_{OH} = –3mA	2.4	3.2		V	MIN
		Buffers	I_{OH} = –15mA	2.0			V	MIN
V_{OL}	Low-level output voltage	Standard[5]	I_{OL} = 4mA		0.25	0.4	V	MIN
			I_{OL} = 8mA		0.25	0.5	V	MIN
		3-State and buffers	I_{OH} = 12mA		0.35	0.4	V	MIN
			I_{OH} = 24mA		0.35	0.5	V	MIN
		–1 version	I_{OH} = 48mA		0.35	0.5	V	4.75V
I_I	Input current at maximum input voltage	Diode inputs	V_{IN} = 7.0V			100	µA	MAX
		PNP inputs	V_{IN} = 7.0V			100	µA	MAX
		Transceiver I/O pins	V_{IN} = 5.5V			100	µA	5.5V
I_{IH}	High–level input current		V_{IH} = 2.7V (20µA × n high U.L.)			n(20)	µA	MAX
I_{IL}	Low–level input current	Diode inputs	V_{IL} = 0.4V (–0.2mA × n low U.L.)			n(–0.2)	µA	MAX
		PNP inputs	V_{IL} = 0.4V (–100µA × n low U.L.)			n(–100)	µA	MAX
I_{OZH}	3-State "off" current high		V_{OUT} = 2.7V			20	µA	MAX
I_{OZL}	3-State "off" current low		V_{OUT} = 0.4V			–20	µA	MAX
I_{OH}	Open collector output leakage		V_{OH} = 5.5V			100	µA	MIN
I_O	Output current[3]		V_O = 2.25V	-30		-112	mA	MAX

Notes to DC electrical characteristics

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_{amb} = +25°C and V_{CC} = 5.0V.
4. MIN and MAX refer to values listed in the data sheets table of recommended operating conditions.
5. Standard refer to the totem–pole pull–up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-State outputs.
6. The output conditions have been chosen to produce current that closely approximates one half of the true short–circuit current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

The AC electrical characteristics Table (see Table 4) contains the guaranteed limits when tested under the conditions set forth in the AC test circuits and waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see table 5) – this is generally the case with counters and flip–flops where setup and hold times are involved.

All of the AC characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transition, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

TABLE 4. AC ELECTRICAL CHARACTERISTICS

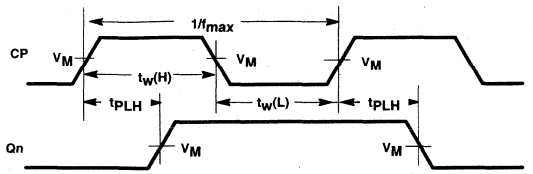
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74ALS373	Waveform 3	2.0 2.0	12.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	3.0 3.0	14.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 6 Waveform 7	2.0 3.0	14.0 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 6 Waveform 7	2.0 2.0	10.0 12.0	ns
f_{max}	Maximum clock frequency	74ALS374	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.0 4.0	12.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 6 Waveform 7	3.0 3.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 6 Waveform 7	2.0 3.0	10.0 12.0	ns

TABLE 5. AC SETUP REQUIREMENTS

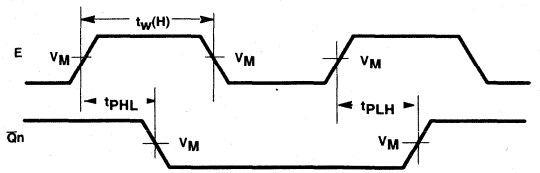
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to E	74ALS373	Waveform 4	6.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to E		Waveform 4	6.0 6.0		ns
t_w (H)	E Pulse width, high		Waveform 1	10.0		ns
t_{su} (H) t_{su} (L)	Setup time, high ort low Dn to CP	74ALS374	Waveform 5	6.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CP		Waveform 5	1.0 1.0		ns
t_w (H) t_w (L)	CP Pulse width, high or low		Waveform 5	10.0 10.0		ns

AC WAVEFORMS

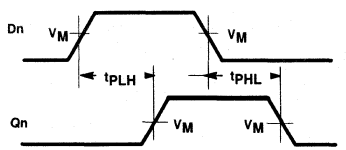
There is no Family Specification for AC Waveforms. Since AC Waveforms vary from device to device, refer to each individual data sheet.



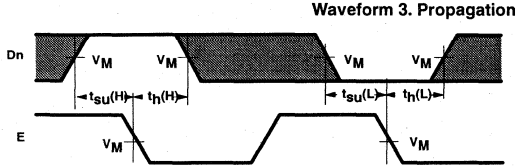
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



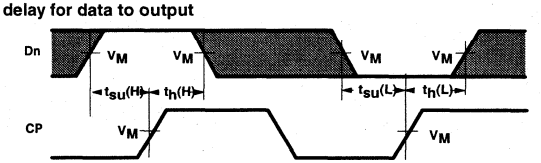
Waveform 2. Propagation delay for enable to output and enable pulse width



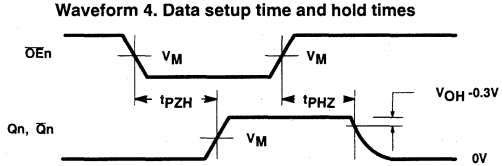
Waveform 3. Propagation delay for data to output



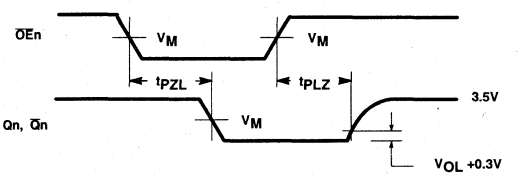
Waveform 4. Data setup time and hold times



Waveform 5. Data setup time and hold times



Waveform 6. 3-State output enable time to high level and output disable time from high level



Waveform 7. 3-State output enable time to low level and output disable time from low level

Figure 1. AC waveforms

Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

The 500 ohm load resistor, R_L to ground, as described in figure 2, acts as a ballast to slightly load the totem–pole pull–up and limit the quiescent high state voltage to about +3.5V. Otherwise, an output would rise quickly to about 3.5V, but then continue to rise very slowly up to about +4.4V. On the subsequent high–to–low transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the low state. Perhaps more importantly, the 500 ohm resistor to ground can be a high frequency, passive probe for a sampling scope, which costs much less than the equivalent high impedance probe. Alternately, the 500ohm load to ground can simply be a 450ohm resistor feeding into a 50 ohm coaxial cable leading to a sampling scope input connector, with the internal 50ohm termination of the scope completing the path to ground. Note that with the internal scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 ohm termination for the pulse generator that supplied the input signal.

Figure 3, test circuit for 3-State outputs, shows a second 500 ohm resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open collector outputs and measuring one set of the enable/disable parameters (low–to–off and off–to–low) of a 3-State output. With the switch closed, the pair of 450 ohm resistors and the +7.0V supply establish a quiescent high level of +3.5V, which correlates with the high level discussed in the preceding paragraph.

As shown in figure 1, AC waveforms, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., low for t_{PLZ} or high for t_{PHZ}).

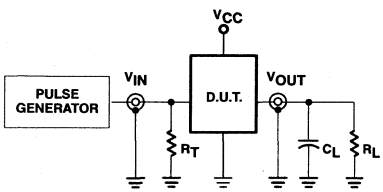
Since the rising or falling waveform is RC controlled, the 0.3V of change is more linear and is less susceptible to external influences.

More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned off. It also gives system designers more realistic

delay times to use in calculating minimum cycle times.

Good, high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize offshoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.0ns, and signal swing of 0V to +3.5V, IMHz square wave is recommended for most propagation delay tests. The repetition test rate must be necessary be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

TEST CIRCUIT AND WAVEFORMS



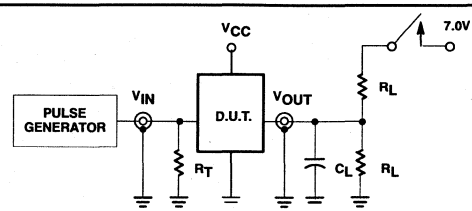
DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 2. Test circuit for totem-pole outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ},	closed
t_{PZL}	closed
OC	open
All other	

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 3. Test circuit for 3–State and open collector (OC) outputs

Data sheet specification guide

INPUT PULSE DEFINITION

The Input Pulse definition defines the input pulse requirements such as pulse amplitude, repetition rate, pulse width, and Transition Time (t_{TLH}, t_{THL}) together with the input pulse waveform.

DC SYMBOLS AND DEFINITIONS FOR VOLTAGES

All voltages are referenced to ground. Negative–voltage limits are specified as absolute values (i.e., –10V is greater than –1.0V).

SYMBOL	PARAMETER	DESCRIPTION
GND	**Ground (Common)**	The reference point from which all voltages in the system are measured. It is the common point to which all other voltage supplies are referenced.
V_{CC}	**Supply voltage**	The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
V_{IK}	**Input clamp voltage**	An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing
V_{IH}	**High–level input voltage**	An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. Note: A minimum is specified that is the least–positive value of high–level input voltage for which operation of the logic element within specification linits is guaranteed.
V_{IL}	**Low–level input voltage**	An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables. Note: A maximum is specified that is the most–positive value of high–level input voltage for which operation of the logic element within specification linits is guaranteed.
V_M	**Measurement voltage**	The reference voltage voltage level on AC waveforms for determining AC performance. Uusally specified as 1.3V for the ALS family
V_{OH}	**High–level output voltage**	The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.
V_{OL}	**Low–level output voltage**	The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.
V_{T+}	**Positive–going threshold voltage**	The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (MIN).
V_{T-}	**Negative–going threshold voltage**	The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+} (MAX).

DC SYMBOLS AND DEFINITIONS FOR CURRENTS

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

SYMBOL	PARAMETER	DESCRIPTION
I_{CC}	**Supply current**	The current into the V_{CC} supply terminal of an integrated circuit.
I_{CCH}	**Supply current, outputs high**	The current into the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at high level.
I_{CCL}	**Supply current, outputs low**	The current into the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at low level.
I_I	**Input current at maximum input voltage**	The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	**High–level input current**	The current[1] into an input when a high–level voltage is applied.
I_{IL}	**Low–level input current**	The current[1] into an input when a low–level voltage is applied.
I_O	**Output current**	The output current that is approximately one half of the true short–circuit output current (I_{OS}).
I_{OH}	**High–level output current**	The current into[1] an output with input conditions applied that, according to the product specification, will establish a high level at the output.
I_{OL}	**Low–level output current**	The current into[1] an output with input conditions applied that, according to the product specification, will establish a low level at the output.
I_{OS}	**Short–circuit output current**	The current into[1] an output when that output is short–circuited to ground (or other specified potential) with input conditions applied to established the output logic level farthest from ground potential (or other specified amount).
I_{OZH}[2]	**Off–state (high impedance–state) output current (of a three–state) with high–level voltage applied**	The current flowing into[1] an output having three–state capability with input conditions established that, according to the production specification, will establish the high–impedance state at the output and with a high–level voltage applied to the output.
I_{OZL}[2]	**Off–state (high impedance–state) output current (of a 3–State) with low–level voltage applied**	The current flowing into[1] an output having three–state capability with input conditions established that, according to the production specification, will establish the high–impedance state at the output and with a low–level voltage applied to the output.

Note to DC symbols and definitions for currents

1. Current out of a terminal is given as a negative value.
2. This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

AC SYMBOLS AND DEFINITIONS

SYMBOL	PARAMETER	DESCRIPTION
f_{max}	**Maximum clock frequency**	The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
t_{PHL}	**Propagation delay time, high–to–low level output**	The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{PHZ}	**Disable time (of a three–state output) from high level**	The time interval between the specified reference points on the input and output voltage waveforms with the three–state output changing from the defined high level to a high–impedance (off) state.
t_{PLH}	**Propagation delay time, low–to–high level output**	The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PLZ}	**Disable time (of a three–state output) from low level**	The time interval between the specified reference points on the input and output voltage waveforms with the three–state output changing from the defined low level to a high–impedance (off) state.
t_{PZH}	**Enable time (of a three–state output) from high level**	The time interval between the specified reference points on the input and output voltage waveforms with the three–state output changing from the defined high level to a high–impedance (off) state.
t_{PZL}	**Enable time (of a three–state output) from low level**	The time interval between the specified reference points on the input and output voltage waveforms with the three–state output changing from the defined low level to a high–impedance (off) state.
t_f	**Fall time**	For a step–function change of the input signal level, the time interval between the end of the delay time (normally 90%), and that instant at which the magnitude of the output signal first passes through a specified value (normally 10%) close to its final value.
t_h[1, 2]	**Hold time**	The time interval during which signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
t_r	**Rise time**	For a step–function change of the input signal level, the time interval between the end of the delay time (normally 10%), and that instant at which the magnitude of the output signal first passes through a specified value (normally 90%) close to its final value.
t_{su}[3, 4]	**Setup time**	The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
t_w	**Pulse duration (width)**	The time interval between specified reference points on the leading and trailing edges of the pulse waveform.
t_{rec}	**Recovery time**	The time interval between reference point on the leading and trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchrnous (clock) pulse input such that the device will respond to the synchronous input.
t_{TLH}	**Transition time, low–to–high level output**	The time interval between a speciified high level voltage and a specified low level voltage on the output voltage waveform with the specified output changing from the defined high level to the defined low level.
t_{THL}	**Transition time, high–to–low level output**	The time interval between a speciified low level voltage and a specified high level voltage on the output voltage waveform with the specified output changing from the defined low level to the defined high level.

Note to AC symbols and definitions

1. The hold time is the actual time interval between two events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longer interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.
3. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
4. The setup time may have a negative value in which case the minimum limit defines the longer interval (between the active transition) for which correct operation of the digital circuit is guaranteed.

THERMAL SYMBOLS AND DEFINITIONS

SYMBOL	PARAMETER	DESCRIPTION
θ_{JA}	**Thermal resistance, junction to ambient**	Thermal resistance between junction to ambeint.
θ_{JC}	**Thermal resistance, junction to case**	Thermal resistance between junction to case.
T_{amb}	**Operating ambient temperature range**	The allowable air temperature range over which the electrical specification of a device are guaranteed
T_C	**Case temperature**	Case temperature of an integrated circuit package
T_J	**Junction temperature**	Temperature at the junction of an integrated circuit.
T_{stg}	**Storage temperature**	Maximum temperature at which device may be stored without damage or performance degradation.

Section 2

Advanced Low-power Schottky Logic (ALS)

CONTENTS

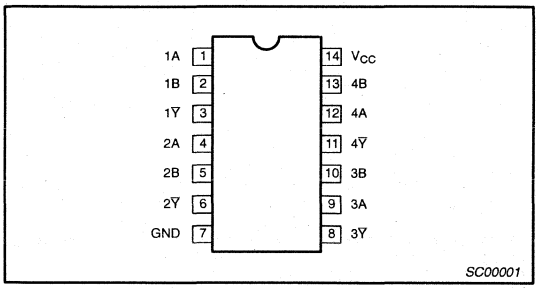
Quad 2-input NAND gate — 74ALS00A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS00A	4.0ns	1.0mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS00AN	SOT27-1
14-pin plastic SO	74ALS00AD	SOT108-1
14-pin plastic SSOP Type II	74ALS00ADB	SOT337-1

PIN CONFIGURATION

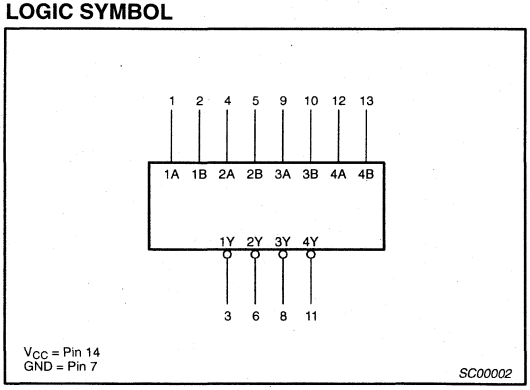


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

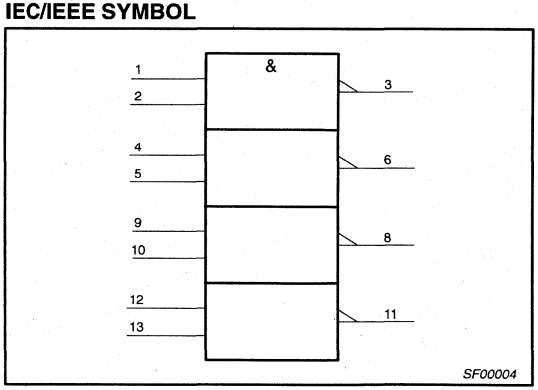
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
n$\overline{Y}$	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

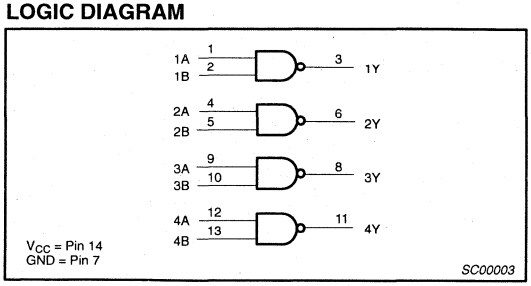
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	n$\overline{Y}$
H	H	L
L	X	H
X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = GND		0.5	0.85	mA
		I_{CCL}		V_I = 4.5V		1.5	3.0	mA

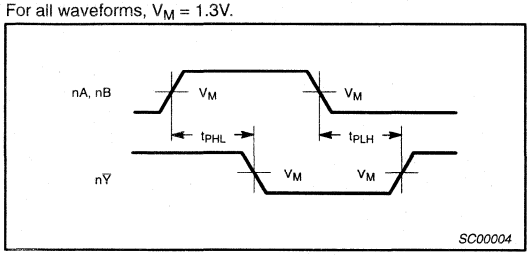
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	Waveform 1	2.0 2.0	11.0 8.0	ns

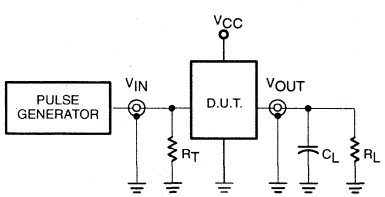
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

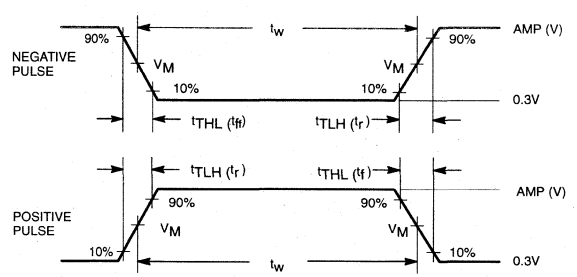


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

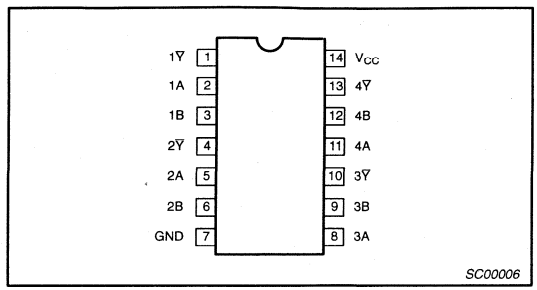
Quad 2-input NOR gate | 74ALS02

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS02	4.0ns	1.0mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS02N	SOT27-1
14-pin plastic SO	74ALS02D	SOT108-1

PIN CONFIGURATION

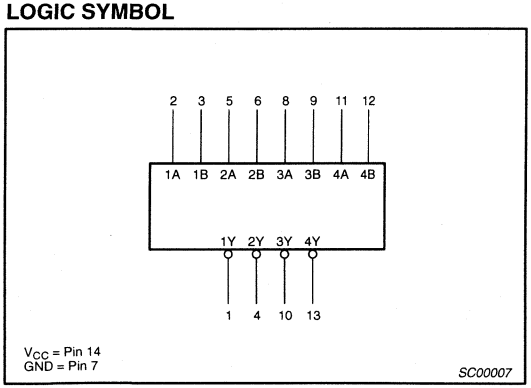


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

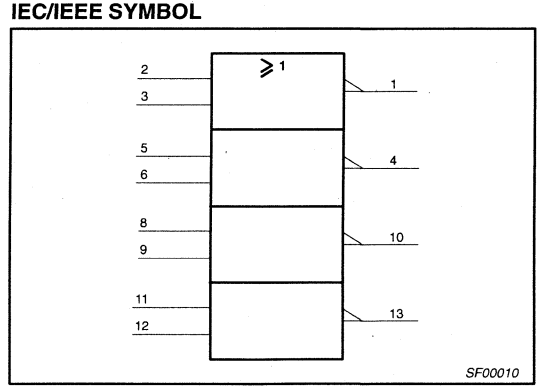
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nȲ	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

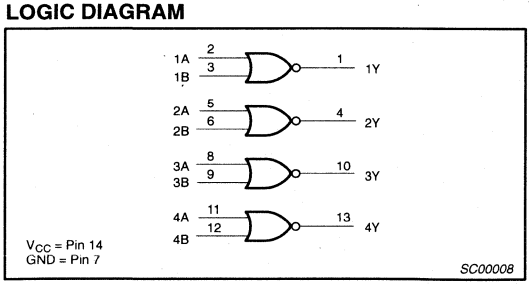
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nȲ
H	H	L
L	X	H
X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–0.4	mA
I_{OL}	Low–level output current			8	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = GND		0.86	2.2	mA
		I_{CCL}		V_I = 4.5V		2.16	4.0	mA

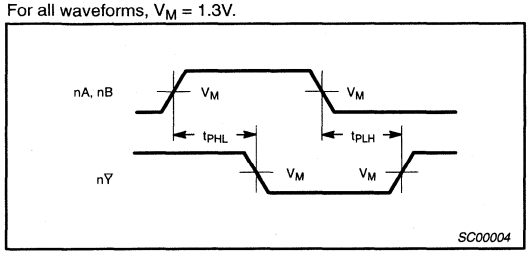
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nȲ	Waveform 1	2.0 2.0	12.0 10.0	ns

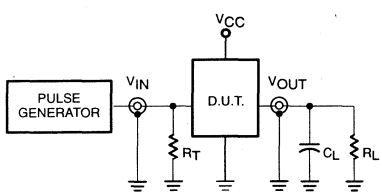
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

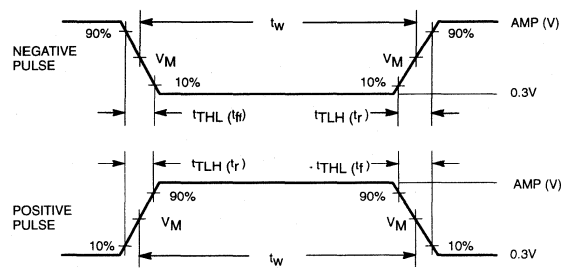


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

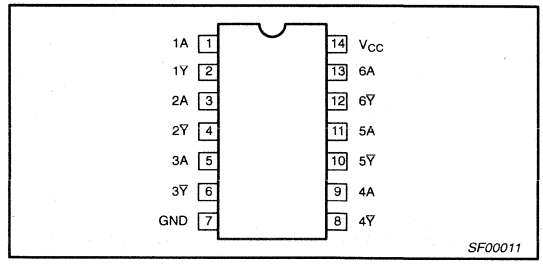
Hex inverter | 74ALS04B

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS04B	3.5ns	2.0mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS04BN	SOT27-1
14-pin plastic SO	74ALS04BD	SOT108-1
14-pin plastic SSOP Type II	74ALS04BDB	SOT337-1

PIN CONFIGURATION

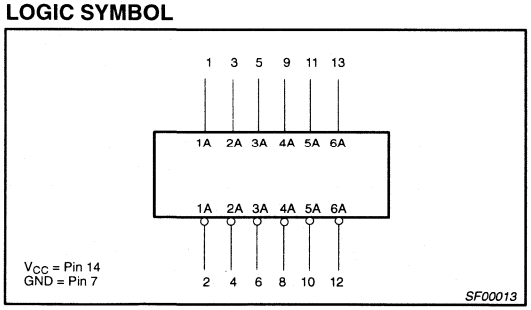


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

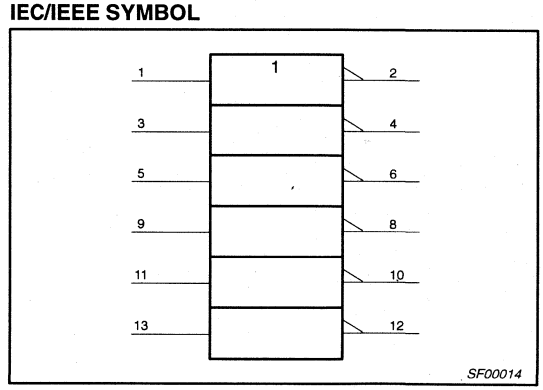
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA	Data input	1.0/1.0	20µA/0.1mA
nȲ	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

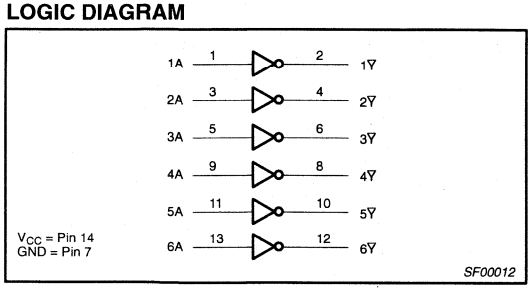
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUT	OUTPUT
nA	nȲ
L	H
H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = GND		0.75	1.1	mA
		I_{CCL}		V_I = 4.5V		3.2	4.2	mA

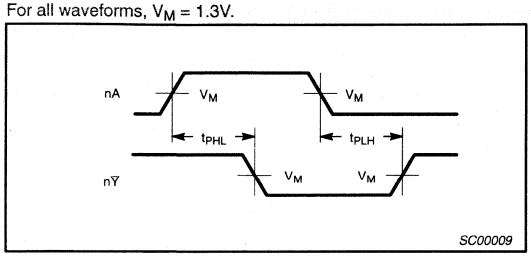
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA to n$\overline{Y}$	Waveform 1	2.0 2.0	11.0 8.0	ns

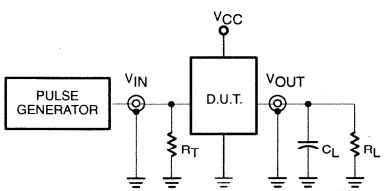
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

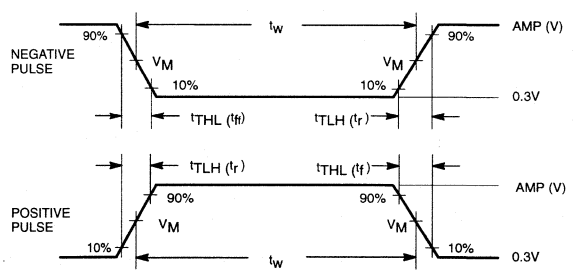


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

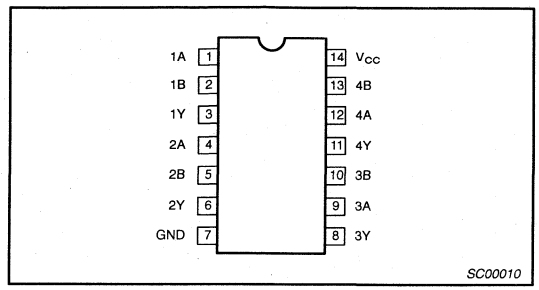
Quad 2-input AND gate | 74ALS08

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS08	5.0ns	1.8mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS08N	SOT27-1
14-pin plastic SO	74ALS08D	SOT108-1
14-pin plastic SSOP Type II	74ALS08DB	SOT337-1

PIN CONFIGURATION



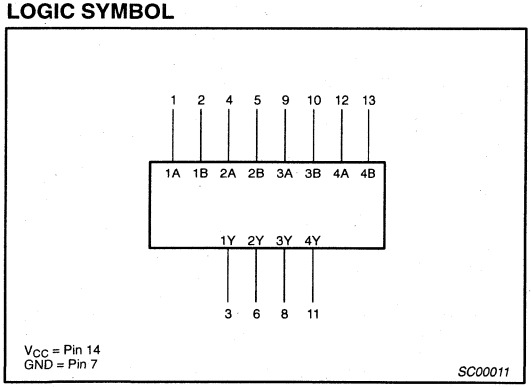
SC00010

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data outputs	20/80	0.4mA/8mA

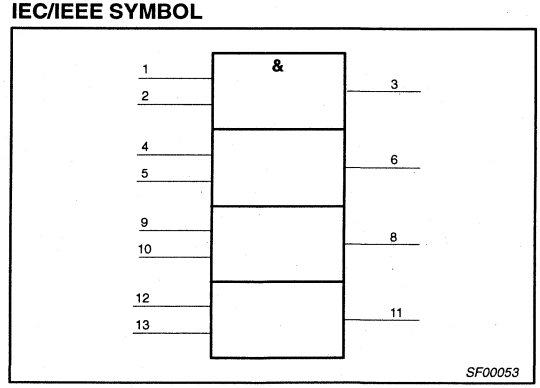
NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



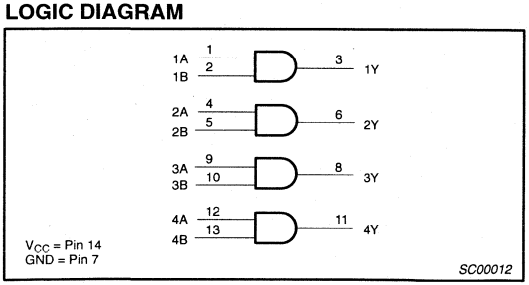
SC00011

IEC/IEEE SYMBOL



SF00053

LOGIC DIAGRAM



SC00012

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nȲ
H	H	L
L	X	H
X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −0.4mA		V_{CC} − 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.3	2.4	mA
		I_{CCL}		V_I = 0V		2.2	4.0	mA

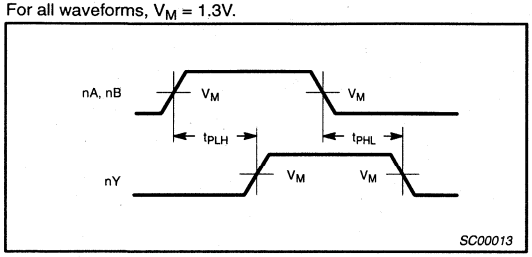
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 1	2.0 3.0	14.0 10.0	ns

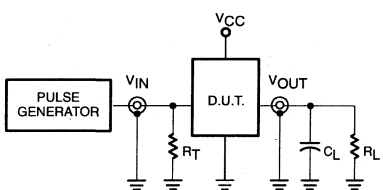
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

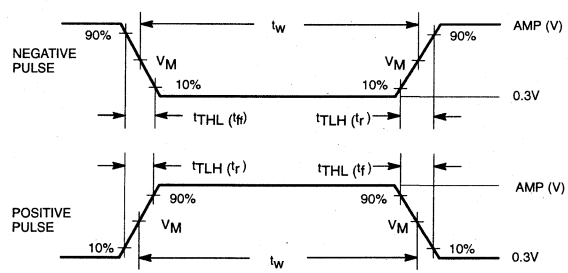


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

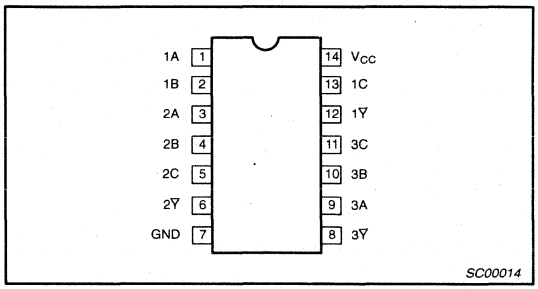
Triple 3-input NAND gate — 74ALS10A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS10A	4.0ns	1.8mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS10AN	SOT27-1
14-pin plastic SO	74ALS10AD	SOT108-1

PIN CONFIGURATION

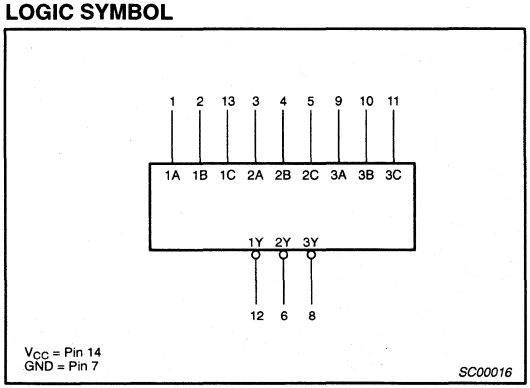


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

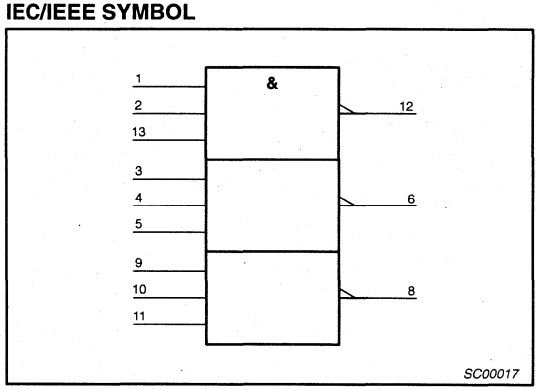
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20µA/0.1mA
nȲ	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

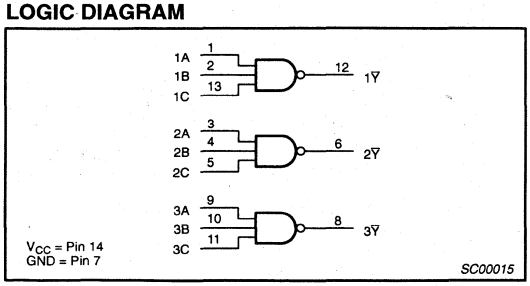
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nȲ
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.5	0.6	mA
		I_{CCL}		V_I = 4.5V		1.6	2.2	mA

NOTES:

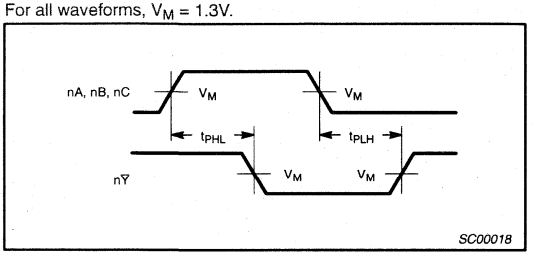
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	Waveform 1	2.0 2.0	11.0 10.0	ns

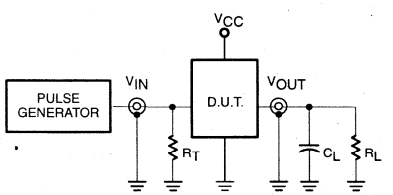
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

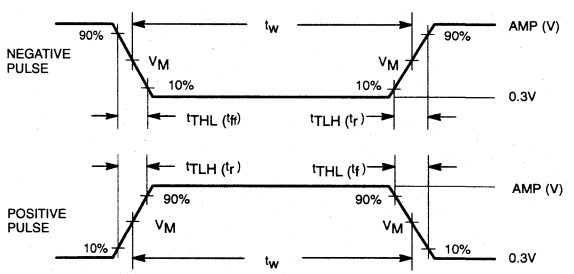


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

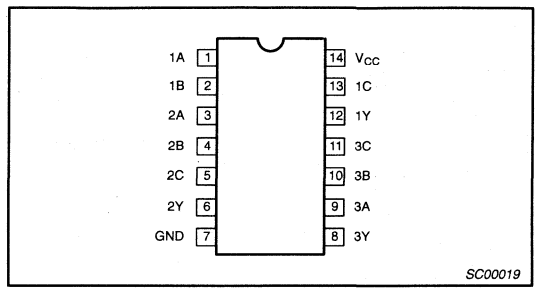
Triple 3-input AND gate | 74ALS11A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS11A	5.5ns	1.3mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS11AN	SOT27-1
14-pin plastic SO	74ALS11AD	SOT108-1

PIN CONFIGURATION

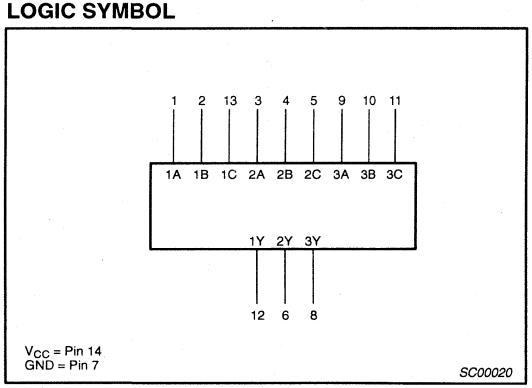


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

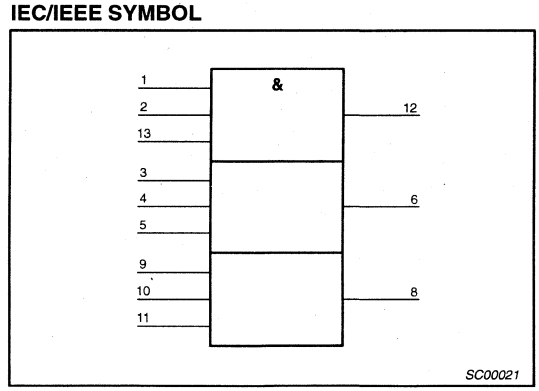
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

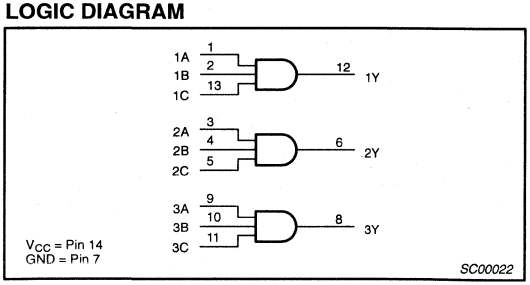
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nB	nY
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −0.4mA		V_{CC} − 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.0	1.8	mA
		I_{CCL}		V_I = 0V		2.0	3.0	mA

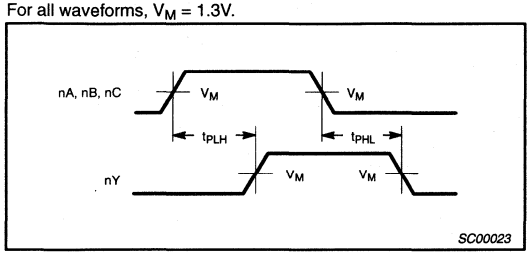
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to nY	Waveform 1	2.0 2.0	11.0 10.0	ns

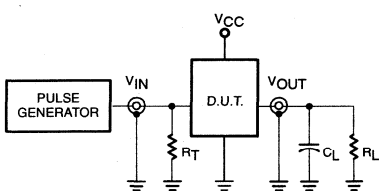
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

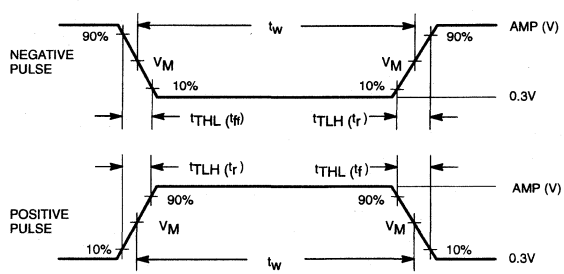


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

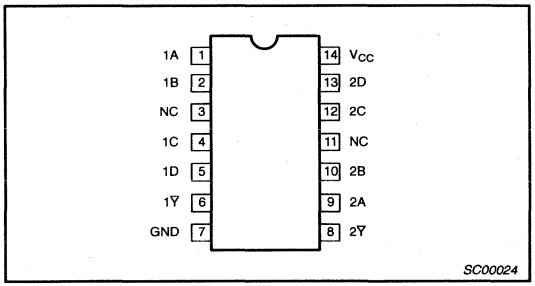
Dual 4-input NAND gate — 74ALS20A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS20A	4.5ns	0.65mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS20AN	SOT27-1
14-pin plastic SO	74ALS20AD	SOT108-1

PIN CONFIGURATION

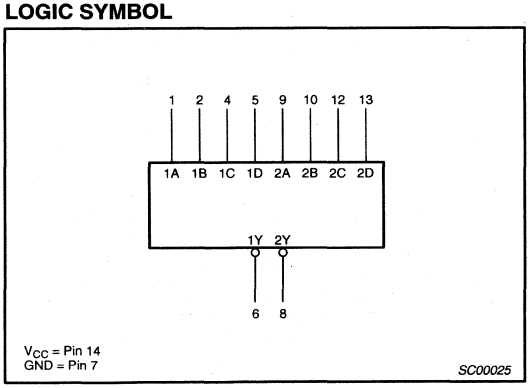


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

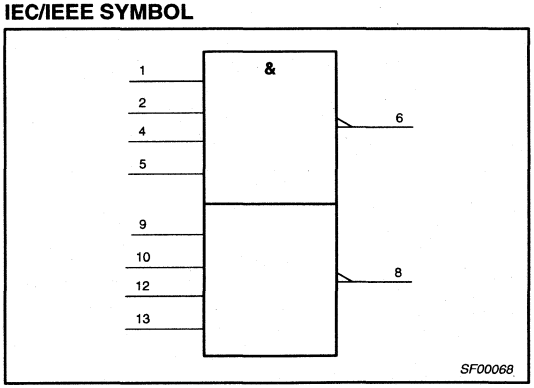
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC, nD	Data inputs	1.0/1.0	20µA/0.1mA
nȲ	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

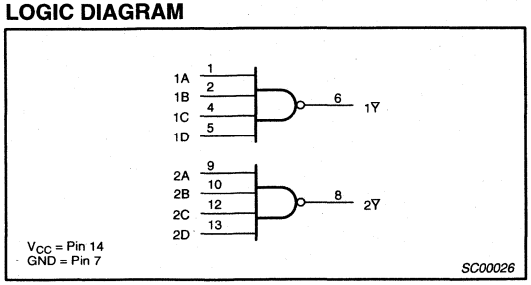
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nȲ
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −0.4mA		V_{CC} − 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.3	0.4	mA
		I_{CCL}		V_I = 4.5V		1.0	1.5	mA

NOTES:

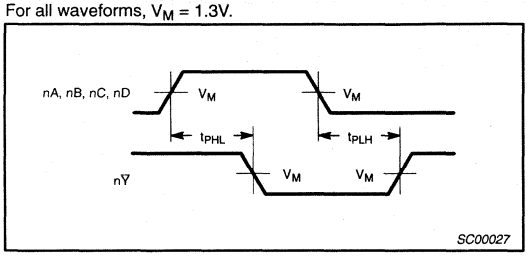
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	Waveform 1	2.0 3.0	11.0 10.0	ns

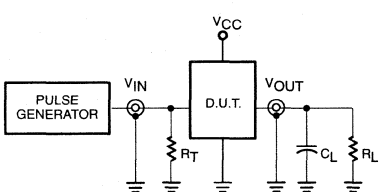
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

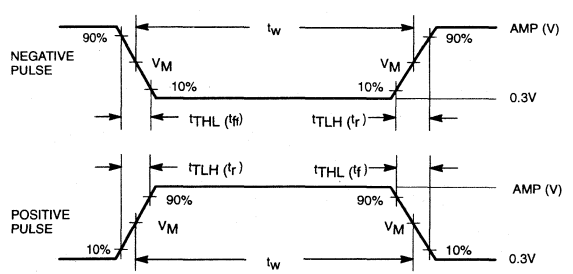


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

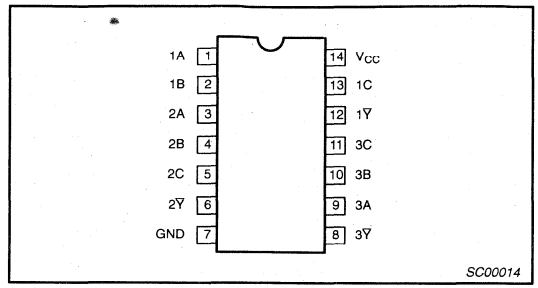
Triple 3-input NOR gate | 74ALS27

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS27	4.0ns	1.5mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS27N	SOT27-1
14-pin plastic SO	74ALS27D	SOT108-1

PIN CONFIGURATION

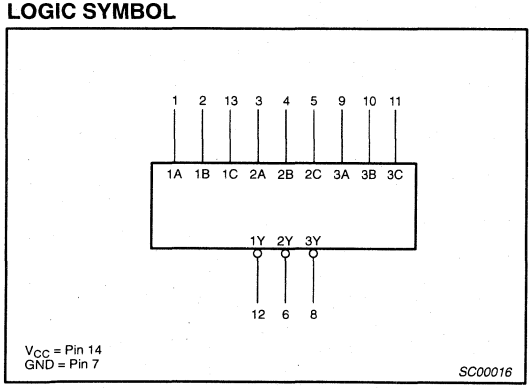


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

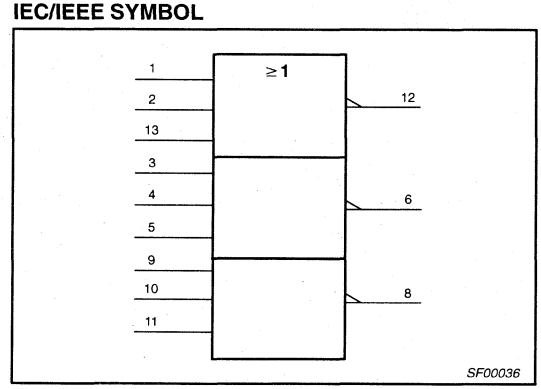
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20µA/0.1mA
nȲ	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

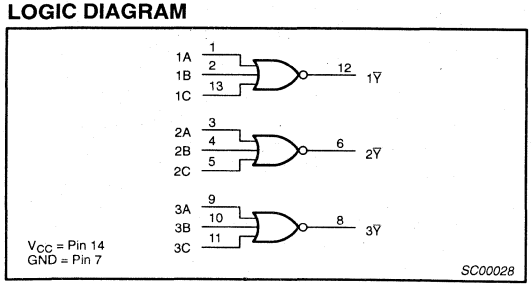
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nȲ
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −0.4mA		V_{CC} − 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		1.0	1.8	mA
		I_{CCL}		V_I = 4.5V		2.0	4.0	mA

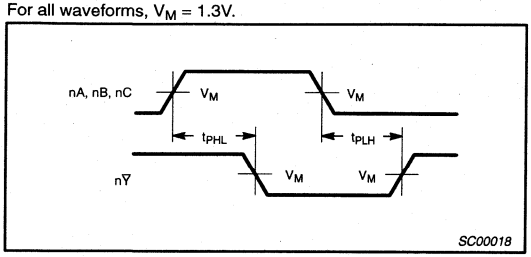
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	Waveform 1	2.0 2.0	15.0 9.0	ns

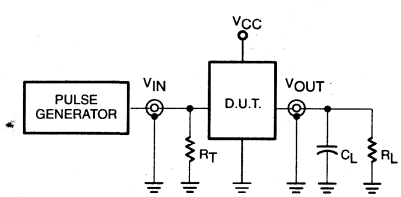
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

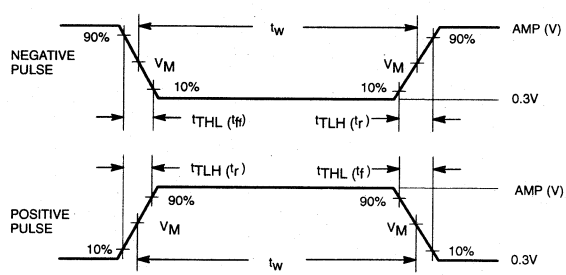


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

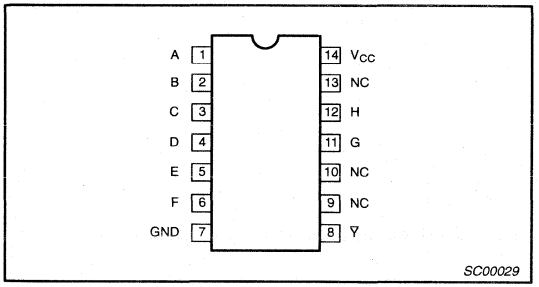
8-input NAND gate | 74ALS30A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS30A	5.0ns	0.5mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS30AN	SOT27-1
14-pin plastic SO	74ALS30AD	SOT108-1

PIN CONFIGURATION

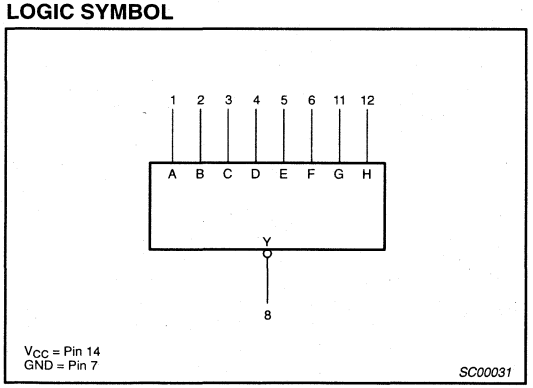


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

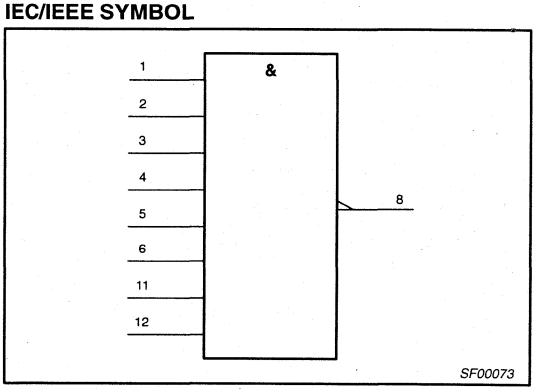
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – H	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{Y}$	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

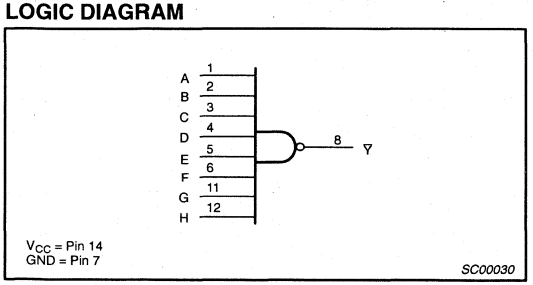
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	$\overline{Y}$
H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–0.4	mA
I_{OL}	Low–level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.20	0.36	mA
		I_{CCL}		V_I = 4.5V		0.64	0.9	mA

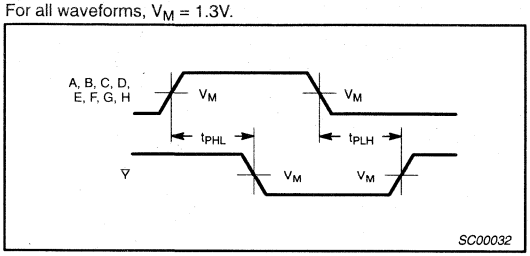
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to n$\overline{Y}$	Waveform 1	2.0 3.0	8.0 10.0	ns

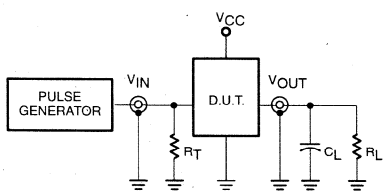
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

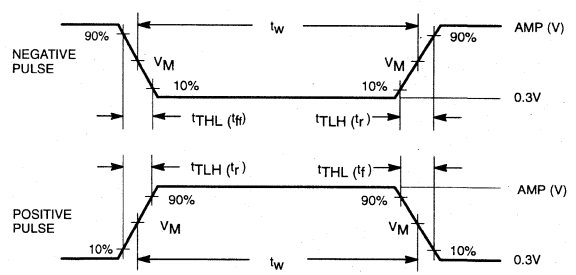


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

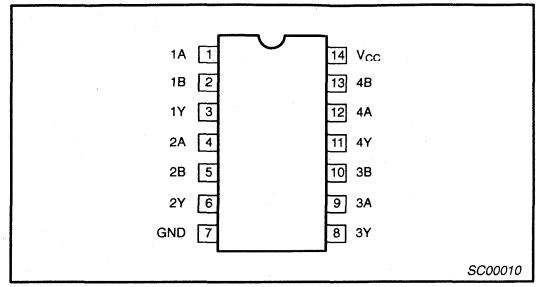
Quad 2-input OR gate — 74ALS32

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS32	5.0ns	2.3mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS32N	SOT27-1
14-pin plastic SO	74ALS32D	SOT108-1
14-pin plastic SSOP Type II	74ALS32DB	SOT337-1

PIN CONFIGURATION

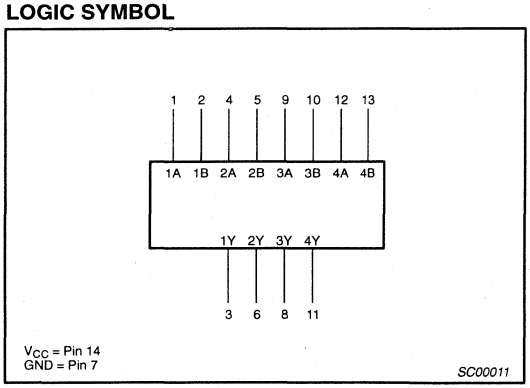


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

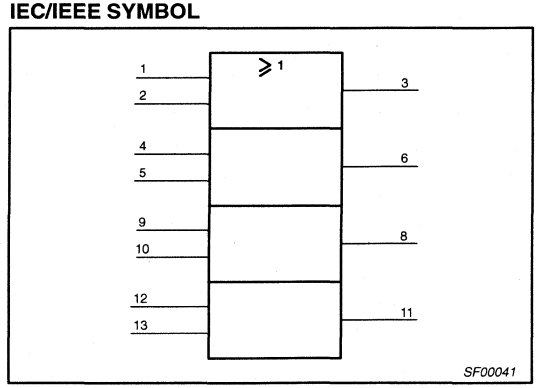
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data output	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

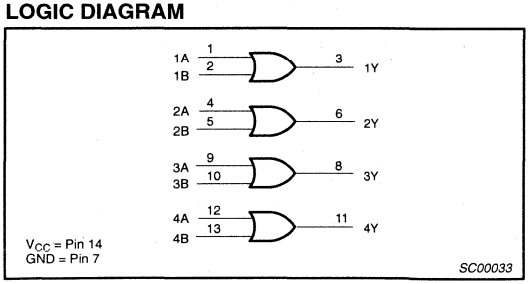
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
H	X	H
X	H	H
L	L	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High–level output current			−0.4	mA
I_{OL}	Low–level output current			8	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −0.4mA		V_{CC} − 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				−0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.6	4.0	mA
		I_{CCL}		V_I = GND		2.8	4.9	mA

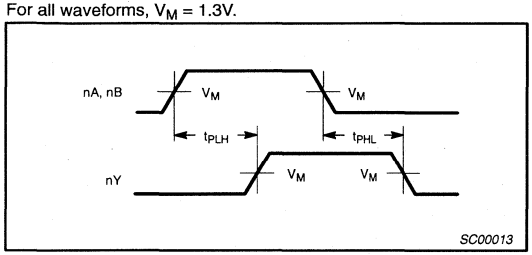
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	Waveform 1	2.0 3.0	14.0 12.0	ns

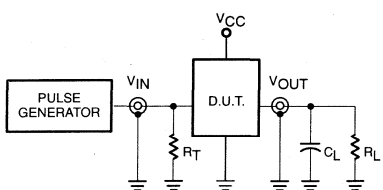
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

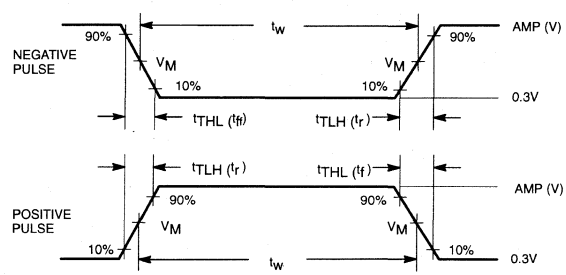


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

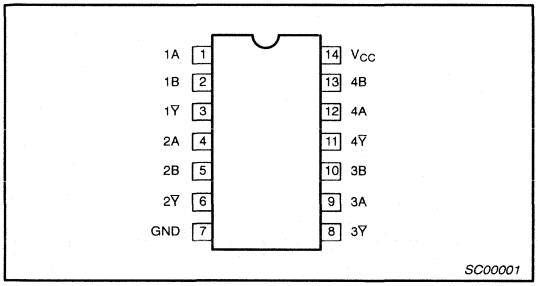
Quad 2-input NAND buffer (open collector) 74ALS38A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS38A	7.0ns	3.5mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14-pin plastic DIP	74ALS38AN	SOT27-1
14-pin plastic SO	74ALS38AD	SOT108-1

PIN CONFIGURATION

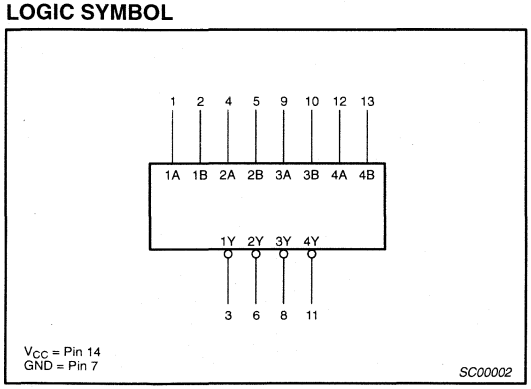


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

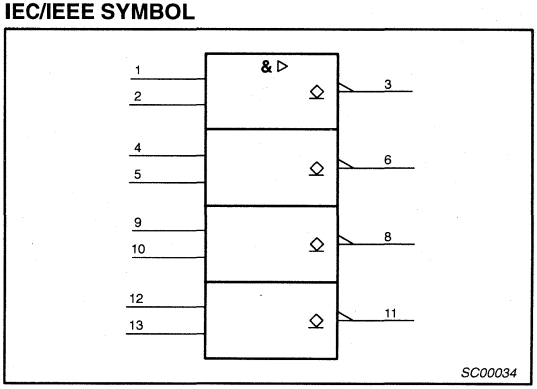
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
n$\overline{Y}$	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

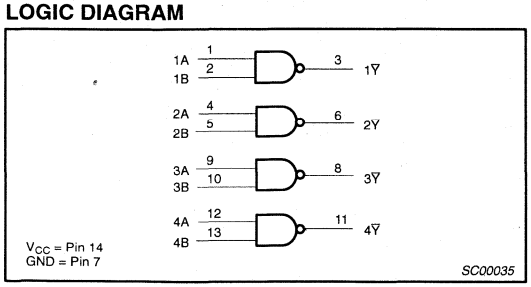
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	n$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				100	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.1	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = GND		0.65	1.6	mA
		I_{CCL}		V_I = 4.5V		6.5	9.0	mA

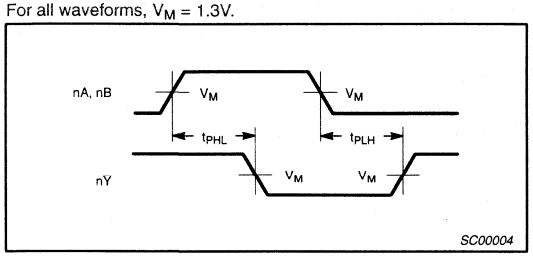
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA or nB to n$\overline{Y}$	Waveform 1	3.0 3.0	11.0 11.0	ns

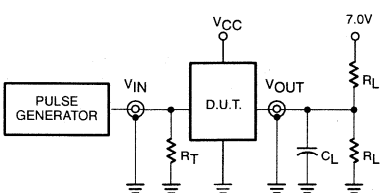
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

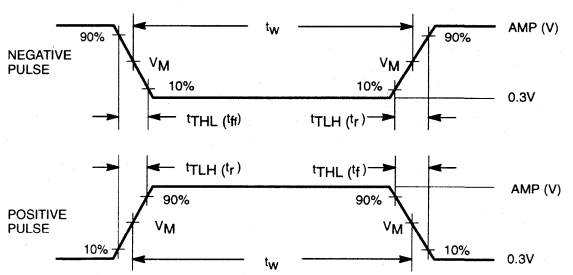


Waveform 1. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00036

Dual D-type flip-flop with set and reset | 74ALS74A

DESCRIPTION

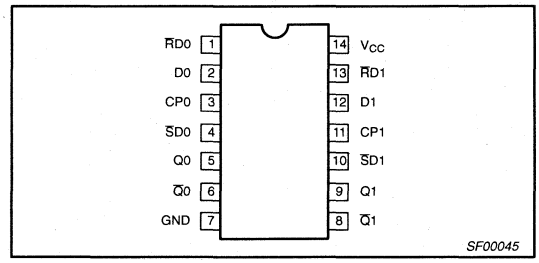
The 74ALS74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active-Low inputs and operate independently of the clock input. When set and reset are inactive (High), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the Low-to-High transition of the clock. Data must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS74A	150MHz	3.0mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
14-pin plastic DIP	74ALS74AN	SOT27-1
14-pin plastic SO	74ALS74AD	SOT108-1
14-pin plastic SSOP Type II	74ALS74ADB	SOT337-1

PIN CONFIGURATION

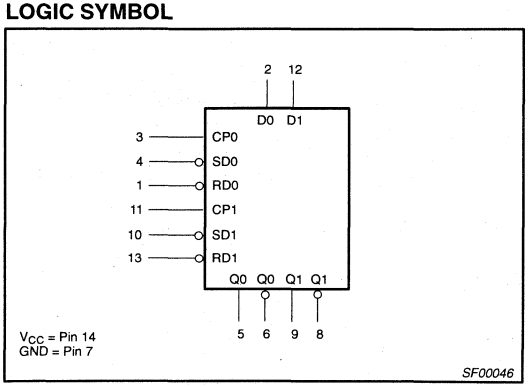


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

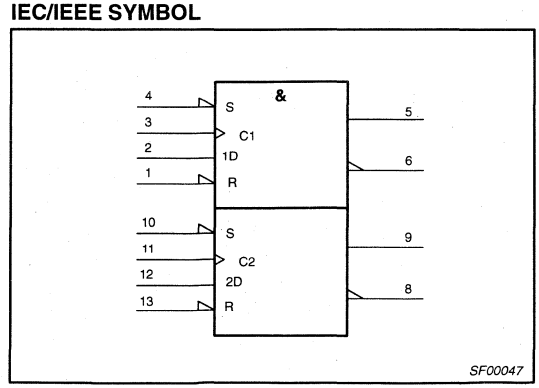
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0, D1	Data inputs	1.0/2.0	20µA/0.2mA
CP0, CP1	Clock inputs (active rising edge)	1.0/2.0	20µA/0.2mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active-Low)	2.0/4.0	40µA/0.4mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active-Low)	2.0/4.0	40µA/0.4mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

LOGIC SYMBOL

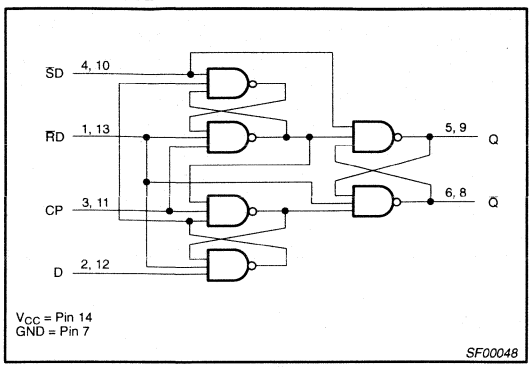


IEC/IEEE SYMBOL



Dual D-type flip-flop with set and reset 74ALS74A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

H = High voltage level
h = High state must be present one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time prior to Low-to-High clock transition
NC= No change from the previous setup
X = Don't care
↑ = Low-to-High clock transition
↕ = Not Low-to-High clock transition
* = Both outputs will be High while both $\overline{SD}$ and $\overline{RD}$ are Low, but the output states are unpredictable if $\overline{SD}$ and $\overline{RD}$ go High simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	Dn, CPn	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		$\overline{S}$Dn, $\overline{R}$Dn					0.2	mA
I_{IH}	High–level input current	Dn, CPn	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{S}$Dn, $\overline{R}$Dn					40	µA
I_{IL}	Low–level input current	Dn, CPn	V_{CC} = MAX, V_I = 0.4V				–0.2	mA
		$\overline{S}$Dn, $\overline{R}$Dn					–0.4	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			3.0	4.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.
4. Measure I_{CC} with the Dn, CPn, and $\overline{S}$Dn grounded, then with Dn, CPn, and $\overline{R}$Dn grounded.

AC ELECTRICAL CHARACTERISTICS

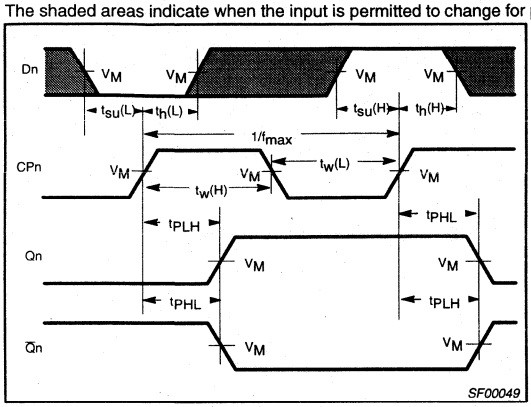
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.0 3.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn or $\overline{R}$D to Qn or $\overline{Q}$n	Waveform 2, 3	1.0 3.0	8.0 10.0	ns

AC SETUP REQUIREMENTS

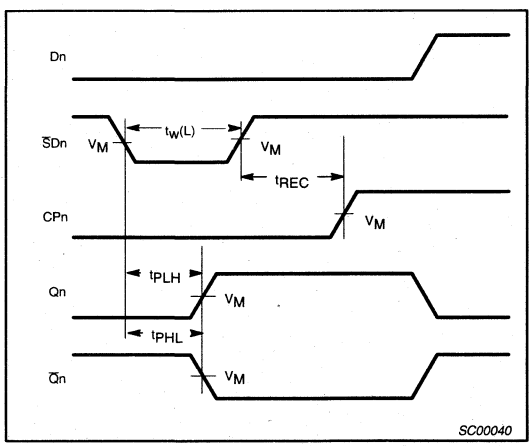
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, High or Low Dn to CPn	Waveform 1	6.0 6.0		ns
t_h (H) t_h (L)	Hold time, High or Low Dn to CPn	Waveform 1	0.0 0.0		ns
t_w (H) t_w (L)	CPn Pulse width High or Low	Waveform 1	6.0 6.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn Pulse width, Low	Waveform 2, 3	6.0		ns
t_{rec}	Recovery time, $\overline{S}$Dn or $\overline{R}$Dn to CPn	Waveform 2, 3	6.0		ns

AC WAVEFORMS

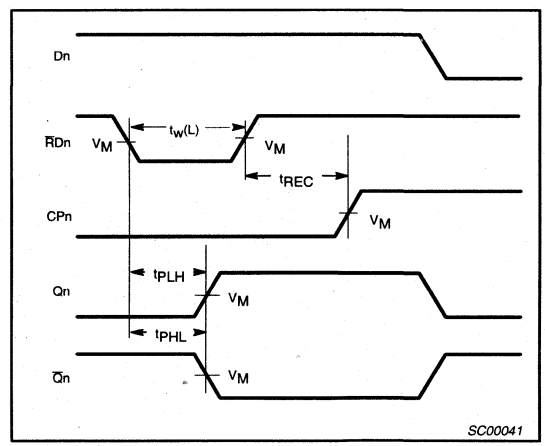
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup and Hold Times, Clock Width, and Maximum Clock Frequency

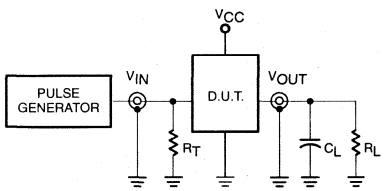


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width and Recovery Time for Set to Clock

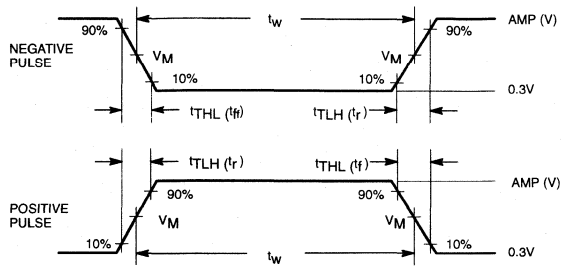


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width and Recovery Time for Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

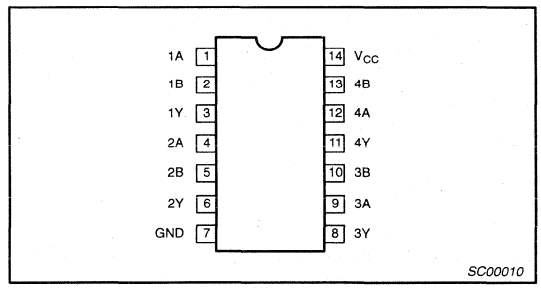
Quad 2-input exclusive-OR gate — 74ALS86

DESCRIPTION

The 74ALS86 contain four independent 2-input Exclusive-OR gates. A common application is a true/complement element. If one input is held Low, the signal on the other input will be reproduced in true form at the output. If one input is held High, the signal on the other input will be reproduced inverted at the output.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS86	6.0ns	3.9mA

PIN CONFIGURATION



ORDERING INFORMATION

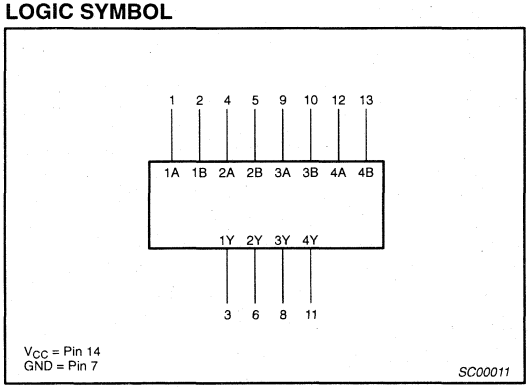
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
14-pin plastic DIP	74ALS86N	SOT27-1
14-pin plastic SO	74ALS86D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

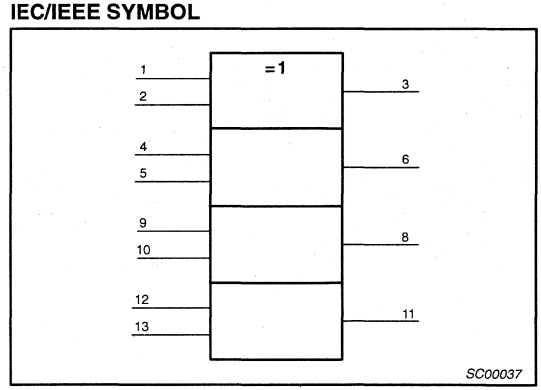
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

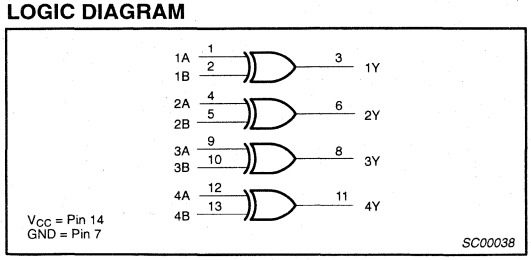
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −0.4mA		V_{CC} − 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, V_I = 4.5V			3.9	5.9	mA

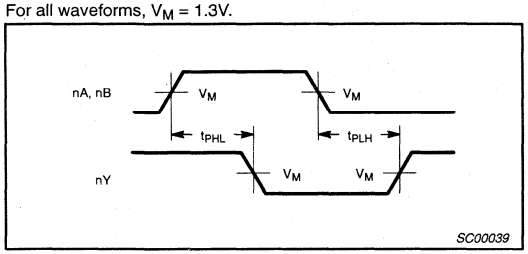
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

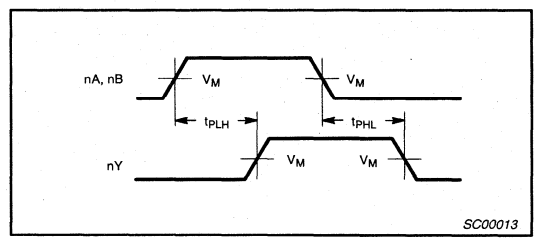
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 2 (other input Low)	2.0 2.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 1 (other input High)	2.0 2.0	12.0 12.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.3V.

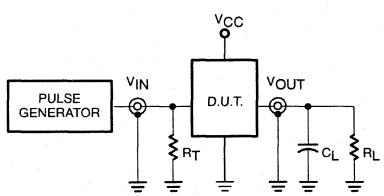


Waveform 1. Propagation Delay for Data to Output

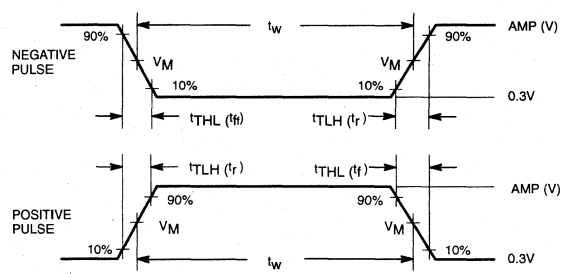


Waveform 2. Propagation Delay for Data to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

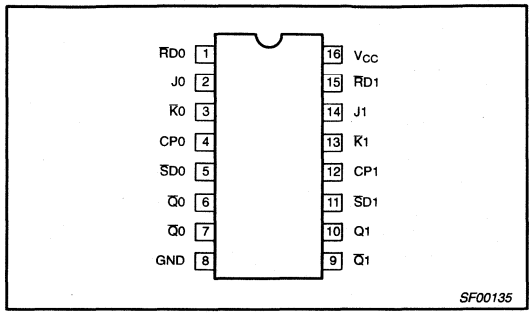
Dual J-$\overline{K}$ positive edge triggered flip-flop with set and reset

74ALS109A

DESCRIPTION

The 74ALS109A is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active-Low inputs and operate independently of the clock (CP) input. The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS109A	150MHz	3.0mA

ORDERING INFORMATION

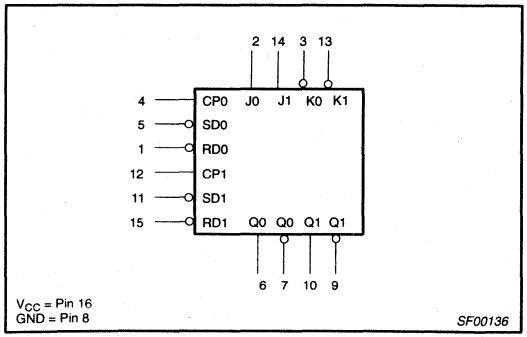
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS109AN	SOT38-4
16-pin plastic SO	74ALS109AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

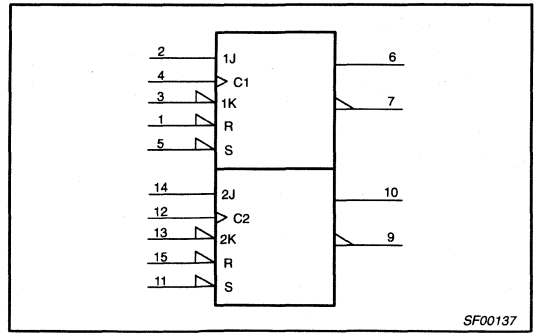
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/2.0	20µA/0.2mA
$\overline{K}$0, $\overline{K}$1	$\overline{K}$ inputs	1.0/2.0	20µA/0.2mA
CP0, CP1	Clock inputs (active rising edge)	1.0/2.0	20µA/0.2mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active-Low)	1.0/4.0	20µA/0.4mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active-Low)	1.0/4.0	20µA/0.4mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



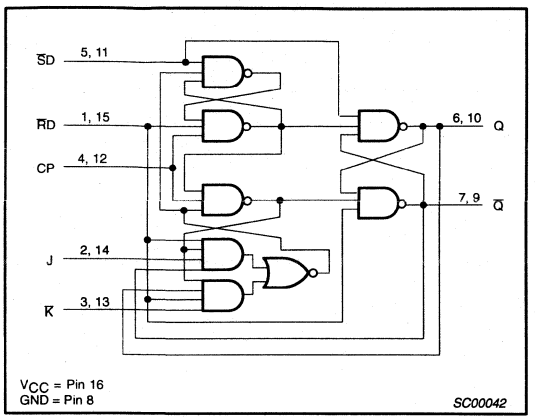
IEC/IEEE SYMBOL



Dual J-$\overline{K}$ positive edge triggered flip-flop with set and reset

74ALS109A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H*	H*	Undetermined*
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0"
H	H	↑	h	h	H	L	Load "1"
H	H	↑	l	h	q	$\overline{q}$	Hold "no change"
H	H	L	l	h	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High state must be present one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time prior to Low-to-High clock transition
q = Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
* = The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the set and reset are near V_{IN} maximum. Furthermore, this configuration is nonstable; that is, it will not remain when either set or reset returns to its inactive (High) level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	Jn, $\overline{K}$n, CPn	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		$\overline{S}$Dn, $\overline{R}$Dn					0.2	mA
I_{IH}	High–level input current	Jn, $\overline{K}$n, CPn	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{S}$Dn, $\overline{R}$Dn					40	µA
I_{IL}	Low–level input current	Jn, $\overline{K}$n, CPn	V_{CC} = MAX, V_I = 0.4V				–0.2	mA
		$\overline{S}$Dn, $\overline{R}$Dn					–0.4	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			3.0	4.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

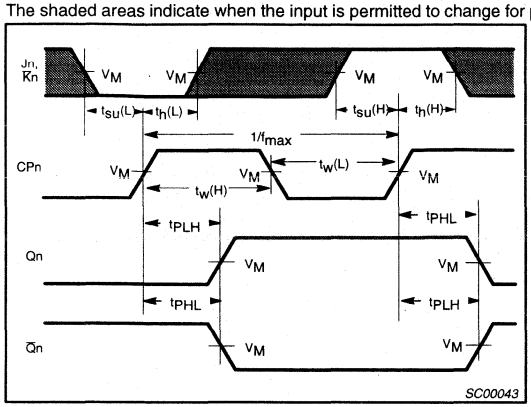
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.0 3.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn or $\overline{R}$D to Qn or $\overline{Q}$n	Waveform 2, 3	1.0 3.0	8.0 10.0	ns

AC SETUP REQUIREMENTS

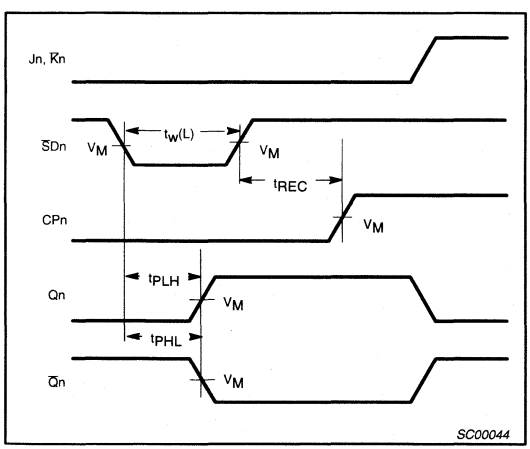
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, High or Low Jn, $\overline{K}$n to CPn	Waveform 1	6.0 6.0		ns
t_h (H) t_h (L)	Hold time, High or Low Jn, $\overline{K}$n to CPn	Waveform 1	0.0 0.0		ns
t_w (H) t_w (L)	CPn Pulse width High or Low	Waveform 1	6.0 6.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn Pulse width Low	Waveform 2, 3	6.0		ns
t_{rec}	Recovery time, $\overline{S}$Dn or $\overline{R}$Dn to CPn	Waveform 2, 3	6.0		ns

AC WAVEFORMS

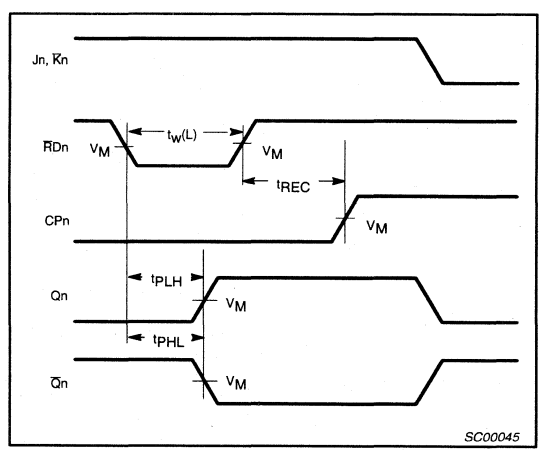
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, Clock Width, and Maximum Clock Frequency

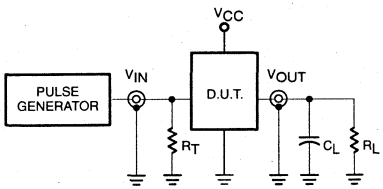


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width and Recovery Time for Set to Clock

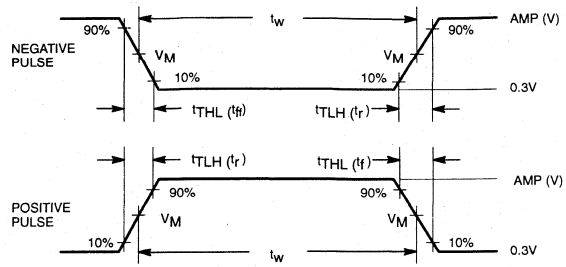


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width and Recovery Time for Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00005

Dual J-K negative edge-triggered flip-flop 74ALS112A

DESCRIPTION

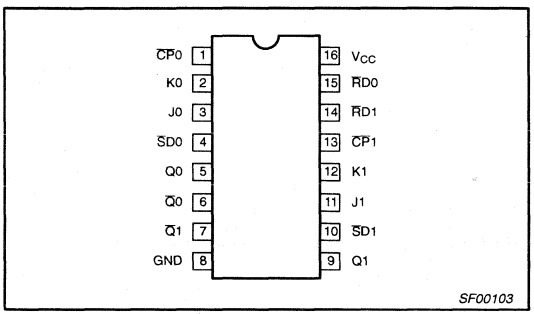
The 74ALS112A, dual negative edge-triggered JK-type flip-flop features individual J, K, clock ($\overline{CP}n$), set ($\overline{SD}$), and reset ($\overline{RD}$) inputs, true (Qn) and complementary ($\overline{Q}n$) outputs.

The $\overline{SD}$ and $\overline{RD}$ inputs, when Low, set or reset the outputs as shown in the function table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}n$ is High and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}n$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS112A	50MHz	3.0mA

PIN CONFIGURATION



ORDERING INFORMATION

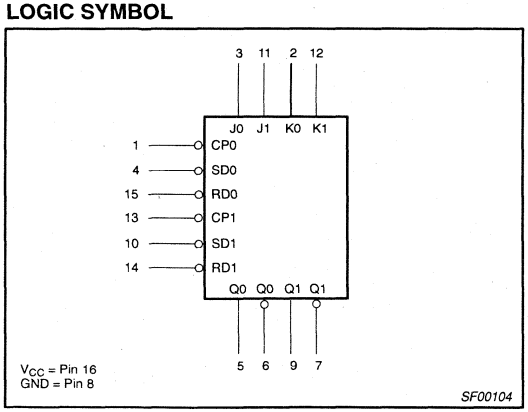
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS112AN	SOT38-4
16-pin plastic SO	74ALS112AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

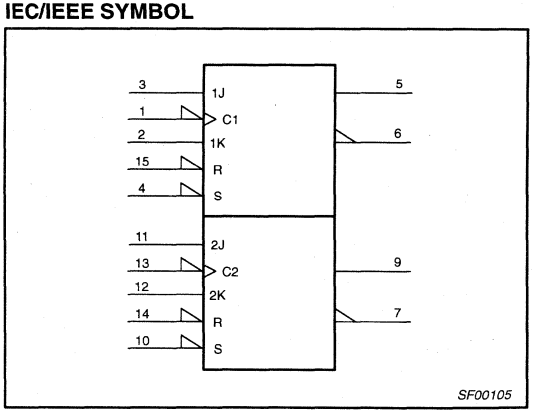
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}$0, $\overline{CP}$1	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.1mA
J0, J1	J inputs	1.0/2.0	20µA/0.2mA
K0, K1	K inputs	1.0/2.0	20µA/0.2mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active-Low)	1.0/2.0	20µA/0.2mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active-Low)	1.0/2.0	20µA/0.2mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

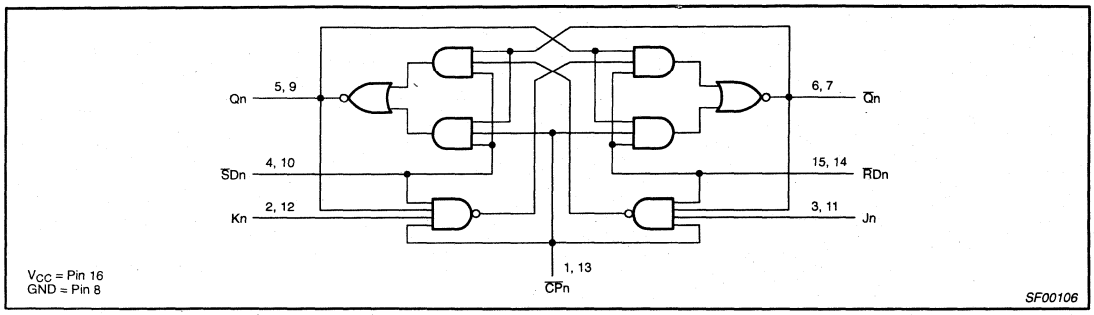
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	$\overline{q}$	q	Toggle
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	h	L	H	Load "0" (Reset)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"
H	H	H	X	X	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High state must be present one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low state must be present one setup time prior to High-to-Low clock transition
q = Lower case indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓ = High-to-Low clock transition
* = Both outputs will be High while both $\overline{SD}$ and $\overline{RD}$ are Low, but the output states are unpredictable if $\overline{SD}$ and $\overline{RD}$ go High simultaneously
Asynchronous inputs: Low input to $\overline{SD}$ sets Q to High level, Low input to $\overline{RD}$ sets Q to Low level. Set and reset are independent of clock. Simultaneous Low on both $\overline{SD}$ and $\overline{RD}$ makes both Q and $\overline{Q}$ High.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 4mA		0.25	0.40	V
			V_{IH} = MIN	I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CP}$n	V_{CC} = MAX, V_I = 0.4V				–0.1	mA
		$\overline{S}$Dn, $\overline{R}$Dn, Jn, Kn					–0.2	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			2.5	4.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

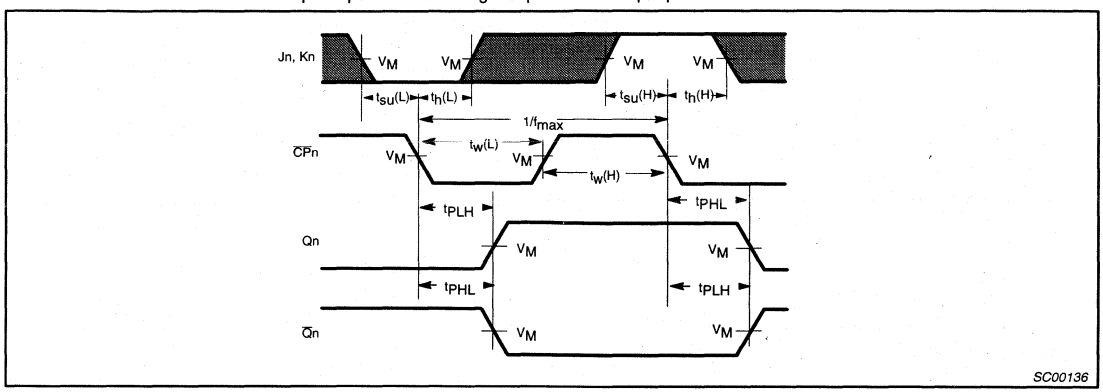
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$n to Qn or $\overline{Q}$n	Waveform 1	2.0 4.0	10.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn or $\overline{R}$D to Qn or $\overline{Q}$n	Waveform 2, 3	1.5 3.5	8.0 9.5	ns

AC SETUP REQUIREMENTS

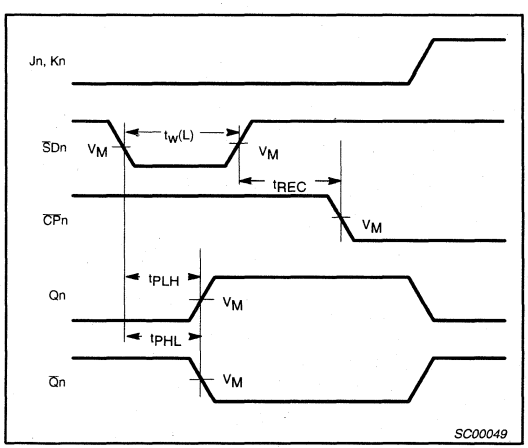
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, High or Low Jn, Kn to $\overline{CP}$n	Waveform 1	8.0 8.0		ns
t_h (H) t_h (L)	Hold time, High or Low Jn, Kn to $\overline{CP}$n	Waveform 1	0.0 0.0		ns
t_w (H) t_w (L)	$\overline{CP}$n Pulse width high or Low	Waveform 1	11.0 8.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn Pulse width Low	Waveform 2, 3	6.0		ns
t_{REC}	Recovery time, $\overline{S}$Dn or $\overline{R}$Dn to $\overline{CP}$n	Waveform 2, 3	8.0		ns

AC WAVEFORMS

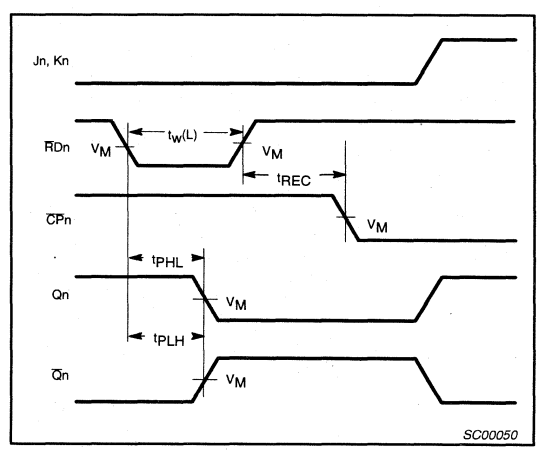
For all waveforms, V_M = 1.3V.
The sahded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, Clock Pulse Width, and Maximum Clock Frequency

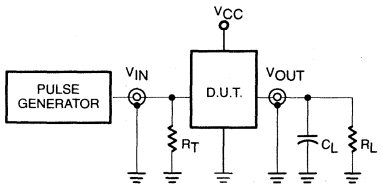


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

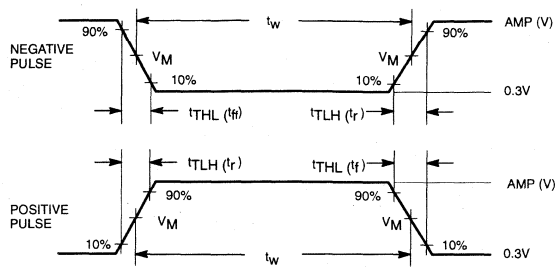


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

1-of-8 decoder/demultiplexer | 74ALS138

FEATURES

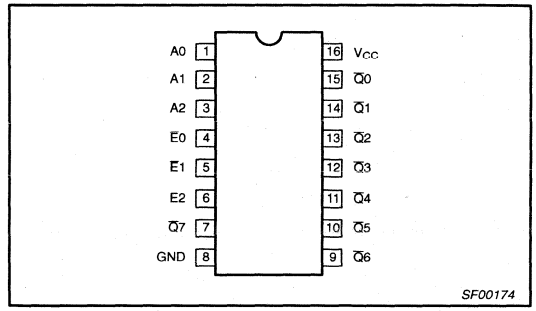
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding

DESCRIPTION

The 74ALS138 decoder accepts three binary weighted inputs (A0, A1, A2) and when enabled, provides eight mutually exclusive, active-Low outputs ($\overline{Q}0 - \overline{Q}7$). The device features three Enable inputs; two active-Low ($\overline{E}0$, $\overline{E}1$) and one active-High (E2). Every output will be High unless $\overline{E}0$ and $\overline{E}1$ are Low and E2 is High. This multiple enable function allows easy parallel expansion of the device to 1-of-32 (5 lines to 32 lines) decoder with just four 74ALS138s and one inverter. The device can be used as an eight output demultiplexer by using one of the active-Low Enable inputs as the data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active-High or active-Low state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS138	12.0ns	4.0mA

PIN CONFIGURATION



ORDERING INFORMATION

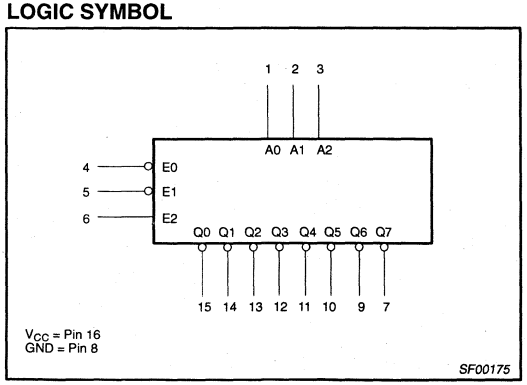
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS138N	SOT38-4
16-pin plastic SO	74ALS138D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

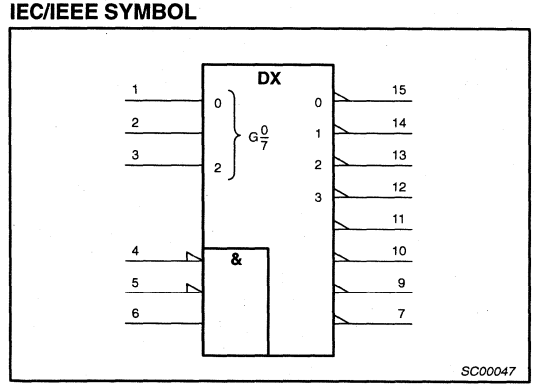
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	Address inputs	1.0/1.0	20µA/0.1mA
$\overline{E}0$, $\overline{E}1$	Enable inputs (active-Low)	1.0/1.0	20µA/0.1mA
E2	Enable input (active-High)	1.0/1.0	20µA/0.1mA
$\overline{Q}0 - \overline{Q}7$	Data outputs (active-Low)	50/33	1.0mA/20mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

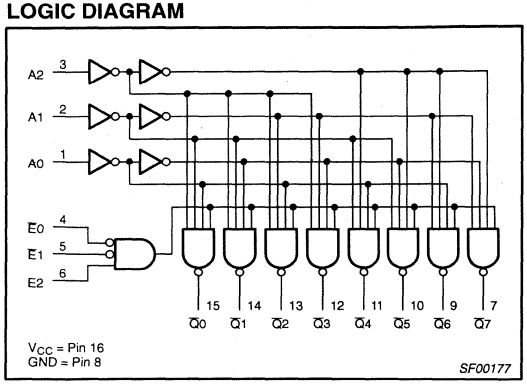
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}0$	$\overline{E}1$	E2	A0	A1	A2	$\overline{Q}0$	$\overline{Q}1$	$\overline{Q}2$	$\overline{Q}3$	$\overline{Q}4$	$\overline{Q}5$	$\overline{Q}6$	$\overline{Q}7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
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L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				−0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			4	7	mA

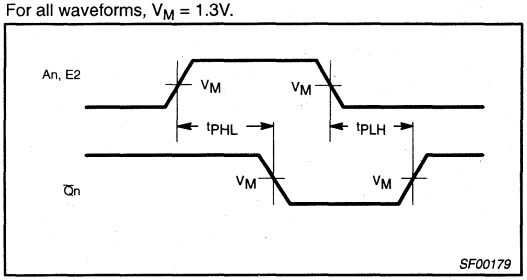
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

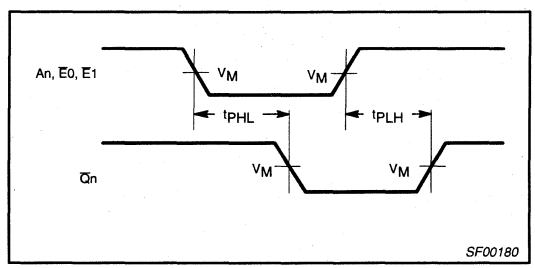
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Qn}$	Waveform 1, 2	3.0 3.0	22.0 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E1}$, $\overline{E2}$ to $\overline{Qn}$	Waveform 2	3.0 3.0	17.0 17.0	ns
t_{PLH} t_{PHL}	Propagation delay E2 to $\overline{Qn}$	Waveform 1	3.0 3.0	17.0 17.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.3V.

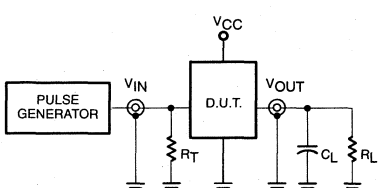


Waveform 1. Propagation Delay for Inverting Outputs

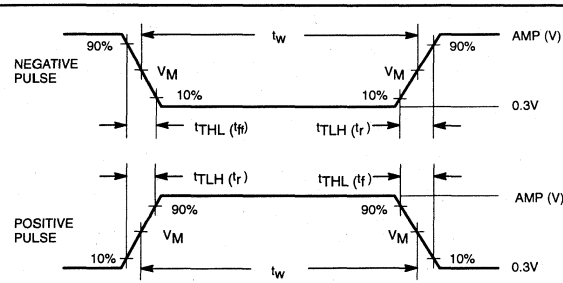


Waveform 2. Propagation Delay for Non-inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Dual 1-of-4 decoder/demultiplexer 74ALS139

FEATURES

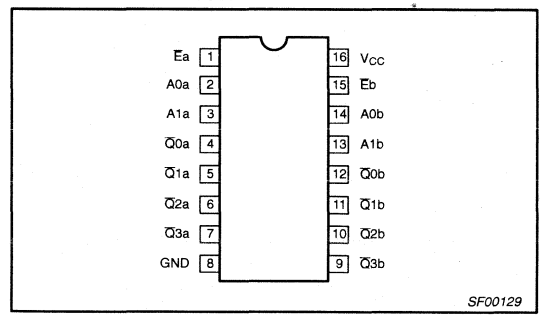
- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multi-function capability

DESCRIPTION

The 74ALS139 is a dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_{0n}, A_{1n}) and providing four mutually exclusive active-Low outputs ($\overline{Q}0n$–$\overline{Q}3n$). Each decoder has an active-Low enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The enable can be used as the data input for a 1-of-4 demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS139	6.0ns	4mA

PIN CONFIGURATION



ORDERING INFORMATION

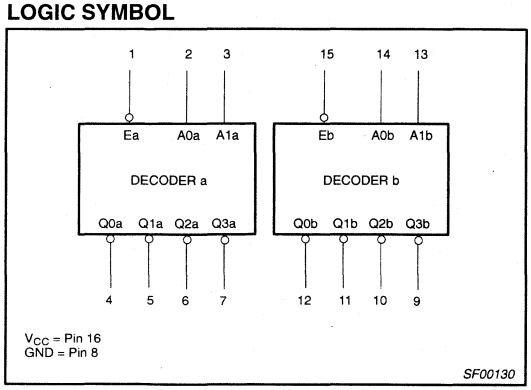
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS139N	SOT38-4
16-pin plastic SO	74ALS139D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

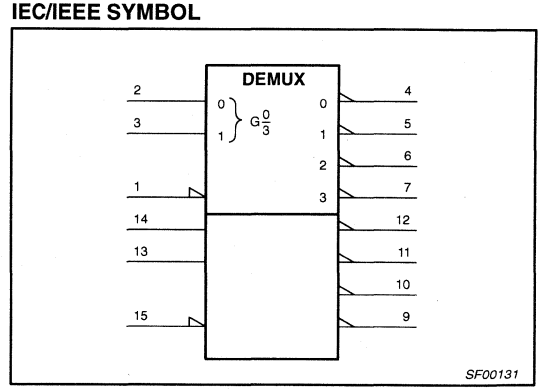
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0n, A1n	Address inputs	1.0/1.0	20µA/0.1mA
$\overline{E}$a, $\overline{E}$b	Enable inputs (active-Low)	1.0/1.0	20µA/0.1mA
$\overline{Q}$0n, $\overline{Q}$1n	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

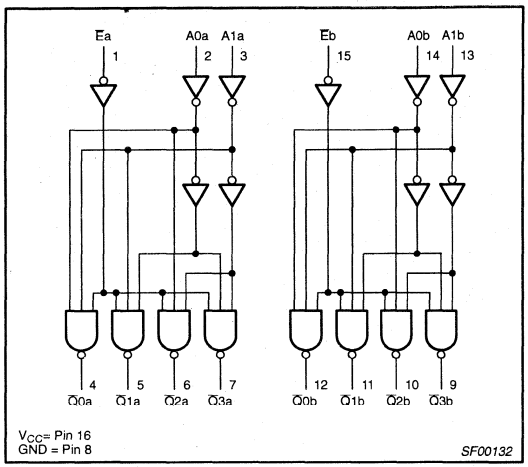
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A0	A1	$\overline{Q}$0	$\overline{Q}$1	$\overline{Q}$2	$\overline{Q}$3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		-30		–112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			4.0	7.0	mA

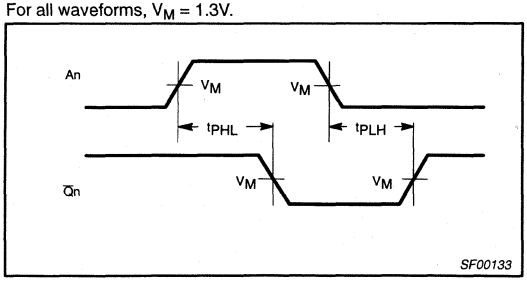
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

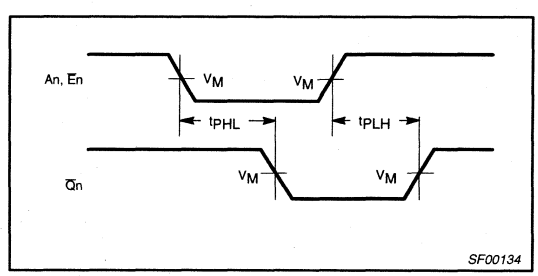
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Q}$n	Waveform 1, 2	3.0 3.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$n to $\overline{Q}$n	Waveform 2	3.0 3.0	8.0 8.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.3V.

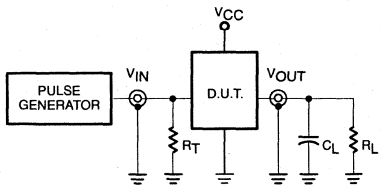


Waveform 1. Propagation Delay for Inverting Outputs

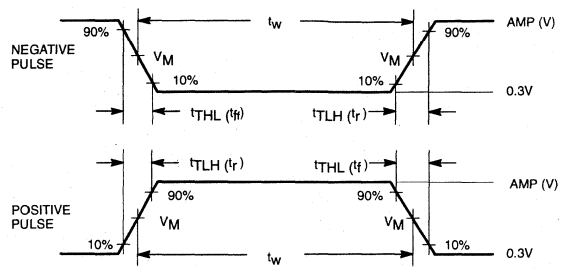


Waveform 2. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

8-input multiplexer 74ALS151

FEATURES

- 8-to-1 multiplexing
- On chip decoding
- Multi-function capability
- Complementary outputs
- See 74ALS251 for 3-State version

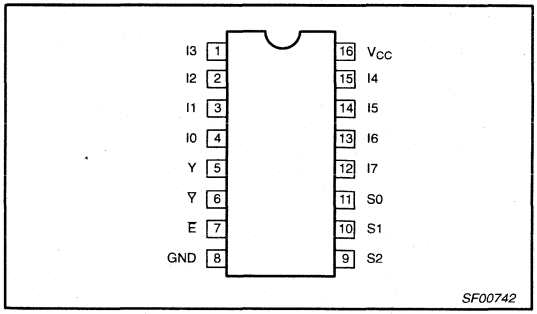
DESCRIPTION

The 74ALS151 is a logic implementation of a single 8-position switch with the switch position controlled by the state of three select (S0, S1, S2) inputs. True (Y) and complementary ($\overline{Y}$) outputs are both provided.

The enable ($\overline{E}$) is active-Low. When $\overline{E}$ is High, Y output is Low and the $\overline{Y}$ output is High regardless of all other inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS151	8.0ns	8.0mA

PIN CONFIGURATION



ORDERING INFORMATION

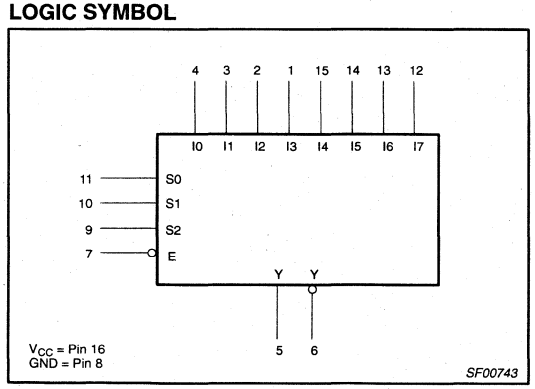
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS151N	SOT38-4
16-pin plastic SO	74ALS151D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

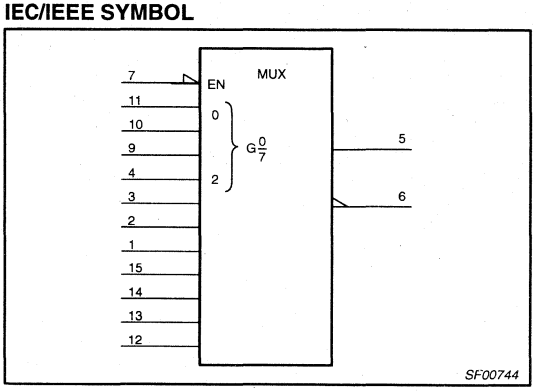
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0 – I7	Data inputs	1.0/1.0	20µA/0.1mA
S0 – S2	Select inputs	1.0/1.0	20µA/0.1mA
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20µA/0.1mA
Y, $\overline{Y}$	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

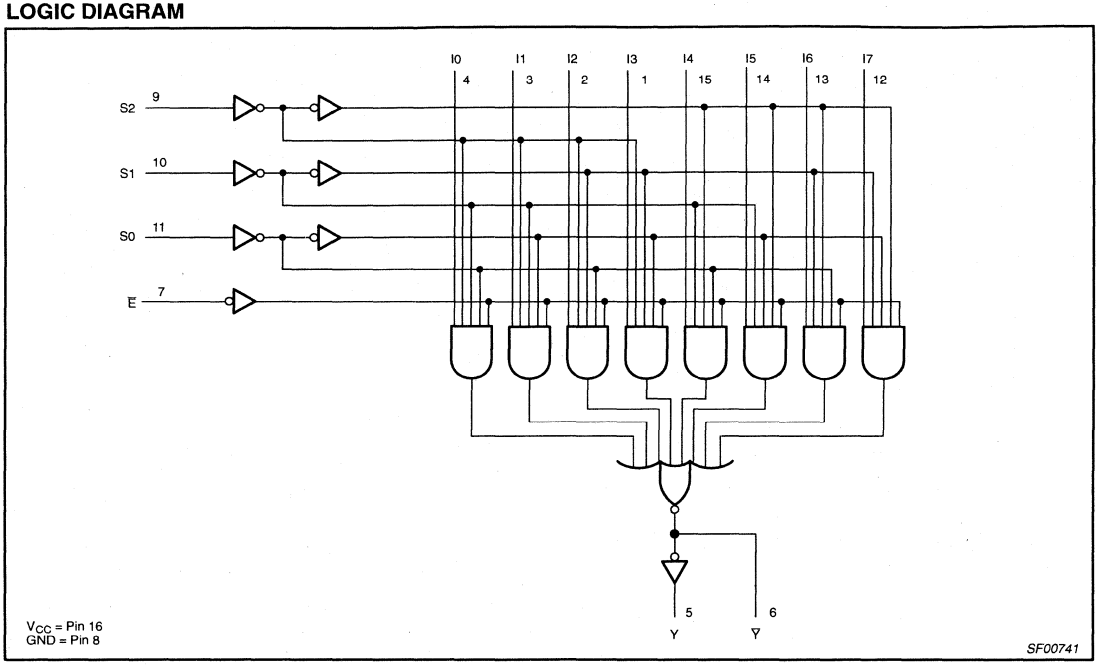
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S2	**S1**	**S0**	**$\overline{E}$**	**Y**	**$\overline{Y}$**
X	X	X	H	L	H
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
			I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
			I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at minimum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				−0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			8.0	12	mA

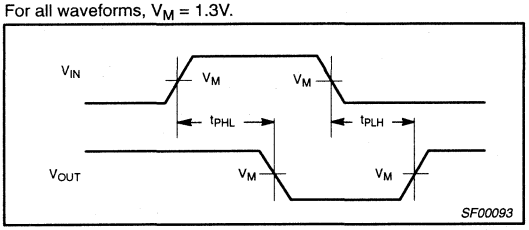
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

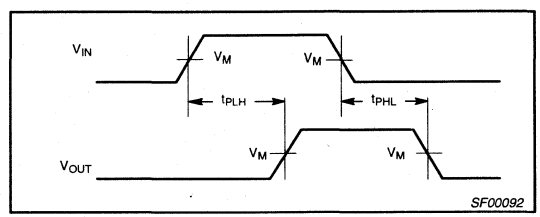
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Y	Waveform 1	3.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay In to $\overline{Y}$	Waveform 2	3.0 5.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Y	Waveform 1, 2	5.0 7.0	15.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to $\overline{Y}$	Waveform 1, 2	5.0 5.0	15.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	Waveform 1	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	Waveform 1	4.0 5.0	12.0 14.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.3V.

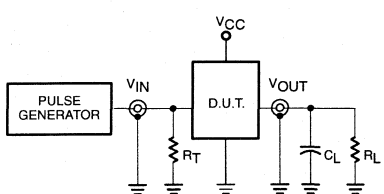


Waveform 1. Propagation Delay for Inverting Output

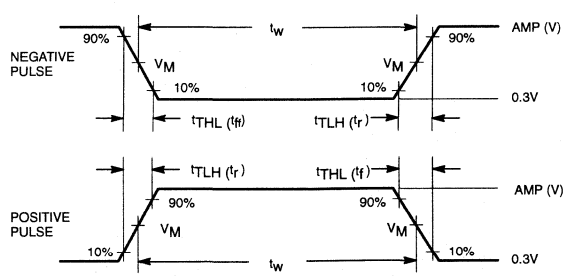


Waveform 2. Propagation Delay for Non-inverting Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Dual 4-input multiplexer | 74ALS153

FEATURES

- Non–inverting outputs
- Common select outputs
- Separate enable for each section
- See 74ALS253 for 3–State version

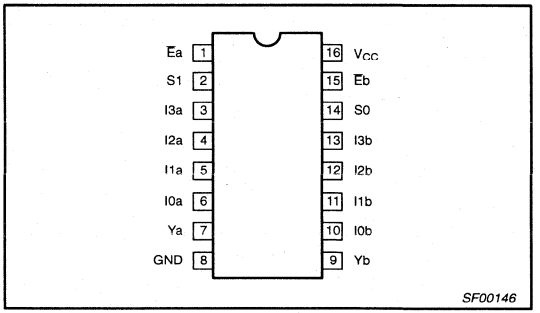
DESCRIPTION

The 74ALS153 has two identical 4–input multiplexer with 3–State outputs which selects two bits of data from four sources by using common select inputs (S0, S1). The two 4–input multiplexer circuits have individual active–Low enables ($\overline{E}a$, $\overline{E}b$) which can be used to strobe the outputs independently. Outputs (Ya, Yb) are forced Low when the corresponding enable is high.

The 74ALS153 is the logic implementation of a 2–pole, 4–position switch where the position of the switch is determined by the logic levels supplied to the common select inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS153	7.0ns	6.5mA

PIN CONFIGURATION



ORDERING INFORMATION

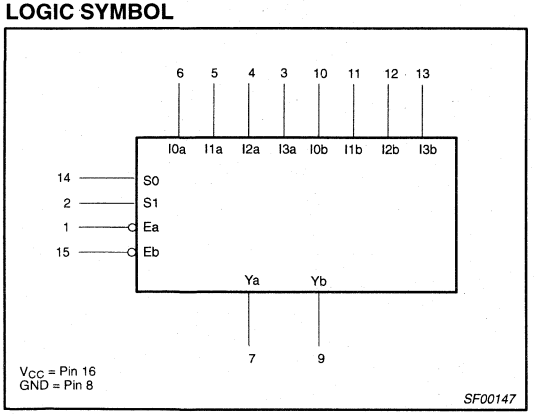
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS153N	SOT38-4
16-pin plastic SO	74ALS153D	SOT109-1
16-pin plastic SSOP Type II	74ALS153DB	SOT338-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

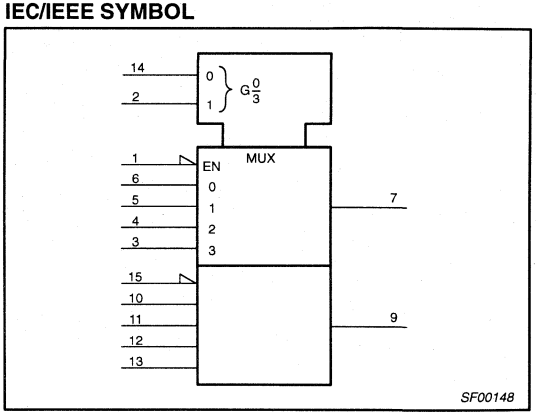
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ioa – I3a	Port A data inputs	1.0/1.0	20µA/0.1mA
Iob – I3b	Port B data inputs	1.0/1.0	20µA/0.1mA
S0, S1	Common select inputs	1.0/1.0	20µA/0.1mA
$\overline{E}a$	Port A enable input	1.0/1.0	20µA/0.1mA
$\overline{E}b$	Port B enable input	1.0/1.0	20µA/0.1mA
Ya, Yb	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

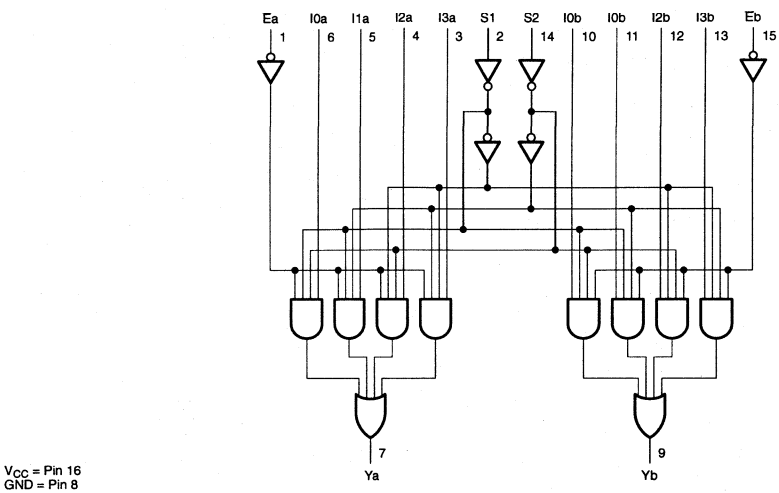
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S0	S1	I0n	I1n	I2n	I3n	$\overline{En}$	Yn
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
			I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
			I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at minimum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				−0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			6.5	12	mA

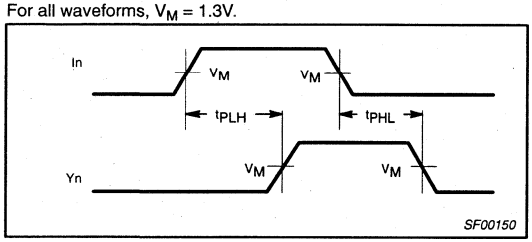
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

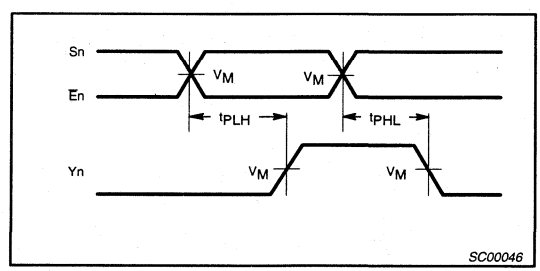
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Yn	Waveform 2	5.0 7.0	15.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{En}$ to Yn	Waveform 2	3.0 5.0	10.0 12.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.3V.

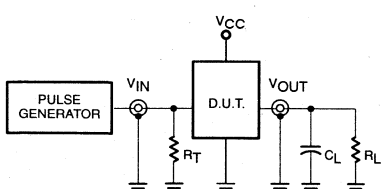


Waveform 1. Propagation Delay for Data to Output

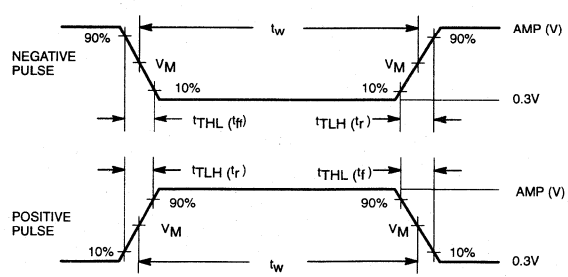


Waveform 2. Propagation Delay for Select or Enable to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Data selector/multiplexer | 74ALS157/74ALS158

74ALS157 Quad 2-input data selector/multiplexer, non-inverting
74ALS158 Quad 2-input data selector/multiplexer, inverting

DESCRIPTION

The 74ALS157 is a quad 2-input multiplexer which selects 4 bits of data from one of two sources under the control of a common select input (S). The enable input ($\overline{E}$) is active when Low. When $\overline{E}$ is High, all of the outputs (Yn) are forced Low regardless of all other input conditions.

Moving data from two registers to a common output bus is a typical use of the 74ALS157. The state of the select input determines the particular register from which data comes.

The device is the logic implementation of 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the select input. The 74ALS158 is similar but has inverting outputs ($\overline{Y}$n).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS157	6.0ns	6mA
74ALS158	6.0ns	6mA

ORDERING INFORMATION

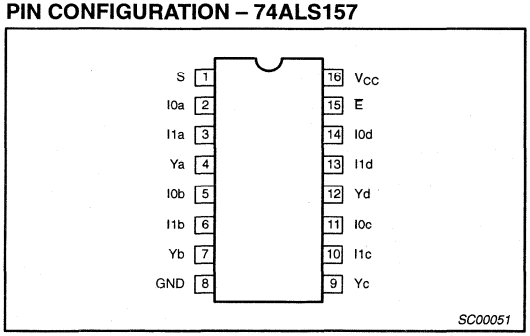
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS157N, 74ALS158N	SOT38-4
16-pin plastic SO	74ALS157D, 74ALS158D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

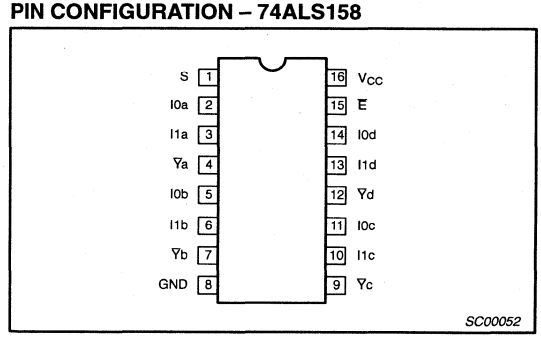
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ina, Inb, Inc, Ind	Data inputs	1.0/1.0	20µA/0.1mA
S	Select input	1.0/1.0	20µA/0.1mA
$\overline{E}$	Enable input	1.0/1.0	20µA/0.1mA
Ya – Yd, $\overline{Y}$a – $\overline{Y}$d	Data outputs	20/240	0.4mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

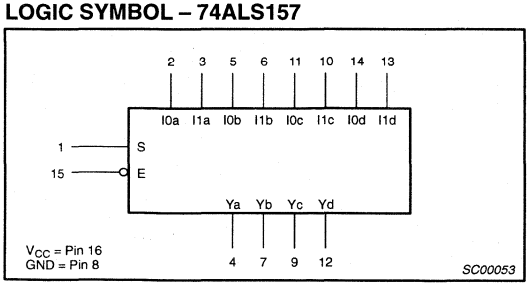
PIN CONFIGURATION – 74ALS157



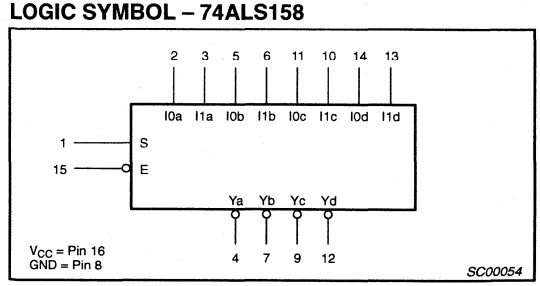
PIN CONFIGURATION – 74ALS158



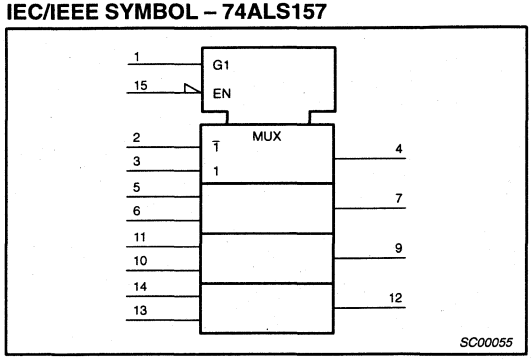
LOGIC SYMBOL – 74ALS157



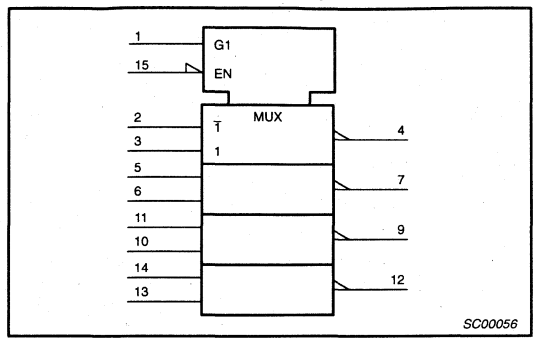
LOGIC SYMBOL – 74ALS158



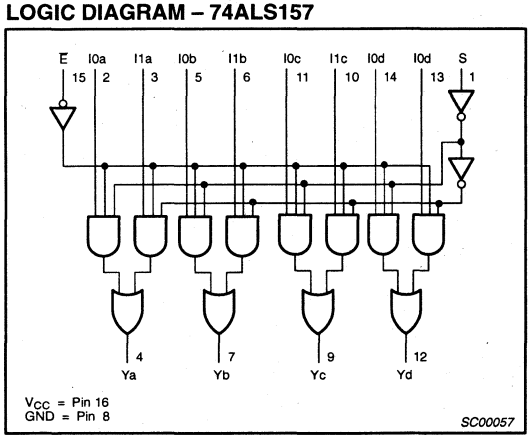
IEC/IEEE SYMBOL – 74ALS157



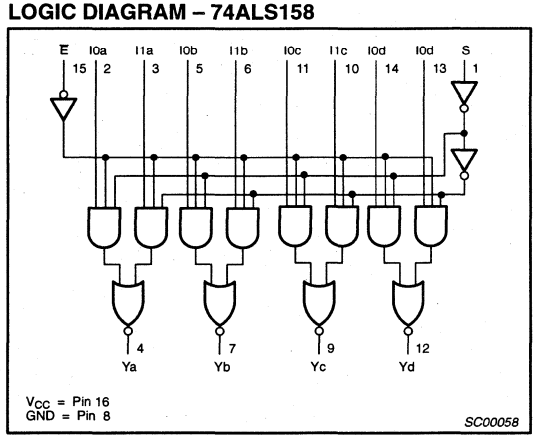
IEC/IEEE SYMBOL – 74ALS158



LOGIC DIAGRAM – 74ALS157



LOGIC DIAGRAM – 74ALS158



FUNCTION TABLE – 74ALS157

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE – 74ALS158

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	$\overline{Y}$n
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	V_{CC} − 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at minimum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				−0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	74ALS157	V_{CC} = MAX			6	11	mA
		74ALS158				6	10	mA

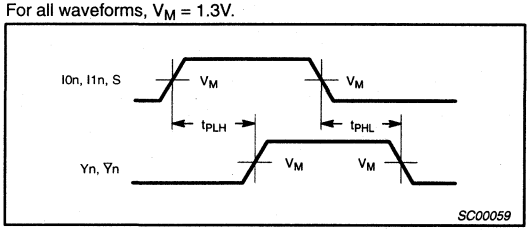
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

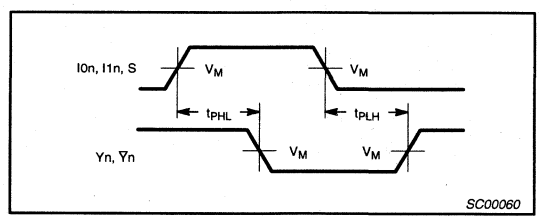
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I0n or I1n to Yn	74ALS157	Waveform 1	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Yn		Waveform 1, 3	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Yn		Waveform 3	4.0 7.0	11.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay I0n or I1n to $\overline{Y}$n	74ALS158	Waveform 2	2.0 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$n		Waveform 2, 4	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$n		Waveform 4	4.0 4.0	14.0 14.0	ns

AC WAVEFORMS

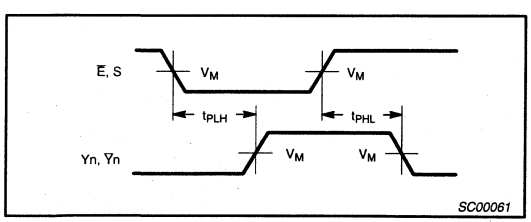
For all waveforms, V_M = 1.3V.



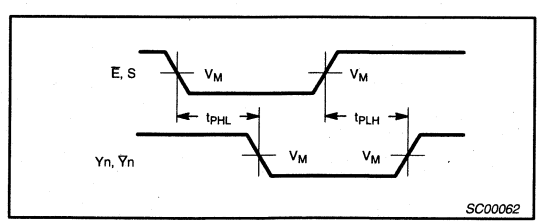
Waveform 1. Propagation Delay for Data and Select to Output



Waveform 2. Propagation Delay for Data and Select to Output

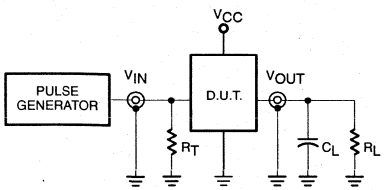


Waveform 3. Propagation Delay for Enable and Select to Output

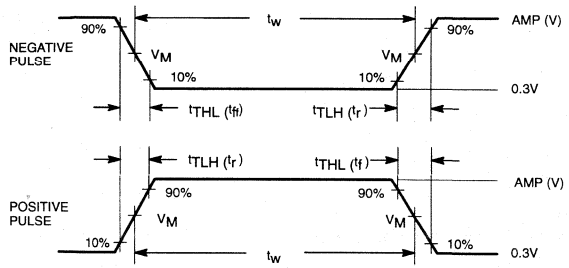


Waveform 4. Propagation Delay for Enable and Select to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

4-bit binary counter 74ALS161B/74ALS163B

74ALS161B 4-bit binary counter, asynchronous reset
74ALS163B 4-bit binary counter, synchronous reset

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset (74ALS161B)
- Synchronous reset (74ALS163B)
- High speed synchronous expansion
- Typical count rate of 140MHz

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS161B	140MHz	10mA
74ALS163B	140MHz	10mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS161BN, 74ALS163BN	SOT38-4
16-pin plastic SO	74ALS161BD, 74ALS163BD	SOT109-1
16-pin plastic SSOP Type II	74ALS161BDB, 74ALS163BDB	SOT338-1

DESCRIPTION

Synchronous presettable 4-bit binary counters (74ALS161B, 74ALS163B) feature an internal carry look-ahead and can be used for high speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the parallel enable ($\overline{PE}$) input disables the counting action and causes the data at the D0 – D3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable (CEP, CET) inputs.

A Low level at the master reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q0 – Q3) in 74ALS161B to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 74ALS163B the clear function is synchronous. A Low level at the synchronous reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q0 – Q3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1).

The carry look-ahead simplifies serial cascading of the counters. Both count enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q0. This pulse can be used to enable the next cascaded stage (see Figure 2).

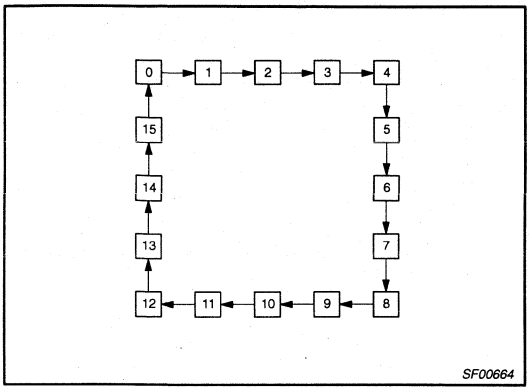
The TC output is subjected to decoding spikes due to internal race conditions, Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.1mA
CEP	Count enable parallel input (active-Low)	1.0/1.0	20µA/0.1mA
CET	Count enable trickle input (active-Low)	1.0/1.0	20µA/0.1mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{PE}$	Parallel enable input (active-Low)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Asynchronous master reset input (active-Low) for 74ALS161B	1.0/1.0	20µA/0.1mA
$\overline{SR}$	Asynchronous reset input (active-Low) for 74ALS163B	1.0/1.0	20µA/0.1mA
Q0 – Q3	Flip-flop outputs	20/80	0.4mA/8mA
TC	Terminal count output (active-Low)	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

STATE DIAGRAM



APPLICATIONS

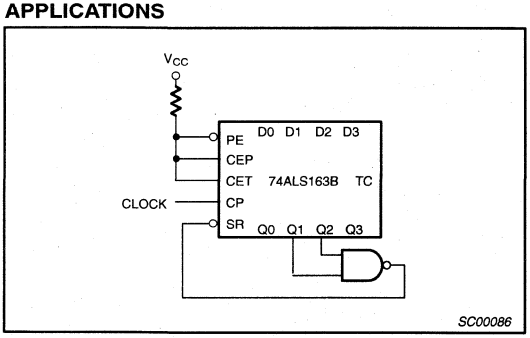


Figure 1. Maximum Count Modifying Scheme
Terminal Count = 6

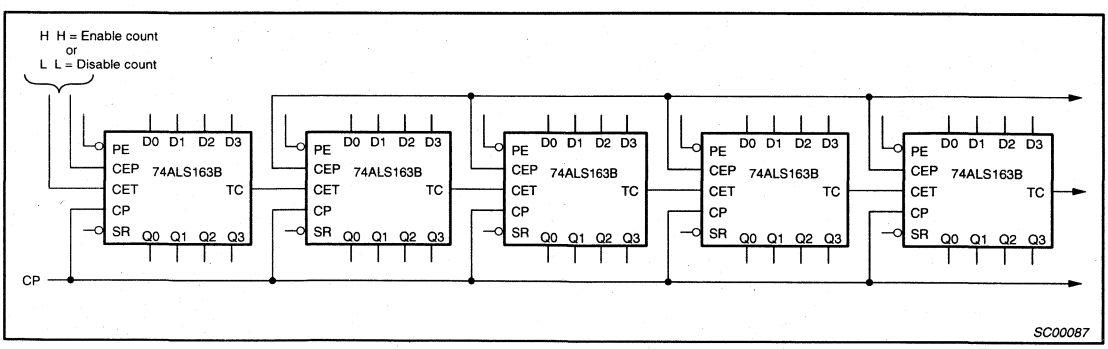
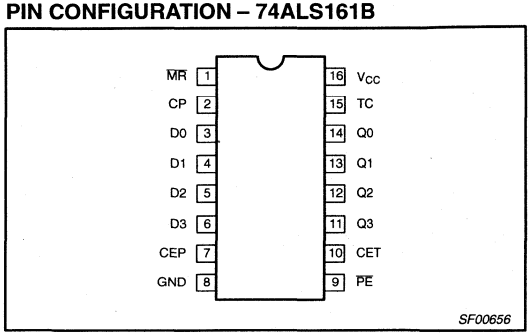
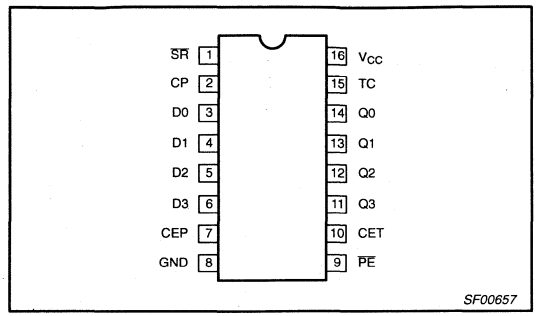


Figure 2. Synchronous Multistage Counting Scheme

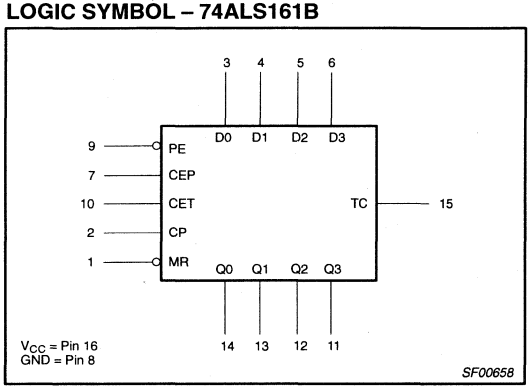
PIN CONFIGURATION – 74ALS161B



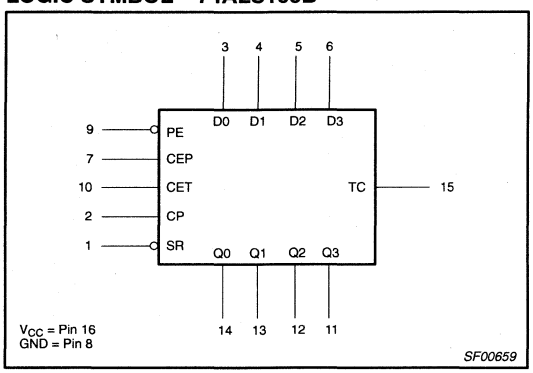
PIN CONFIGURATION – 74ALS163B



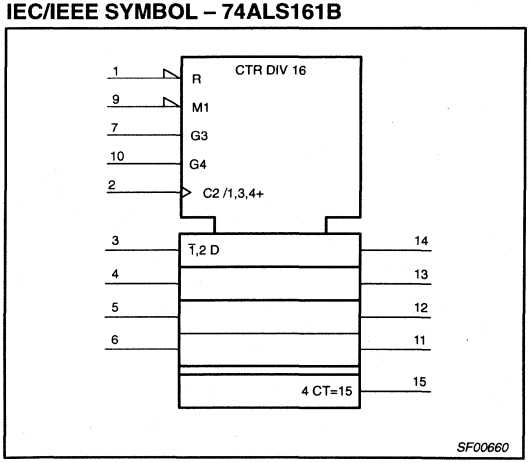
LOGIC SYMBOL – 74ALS161B



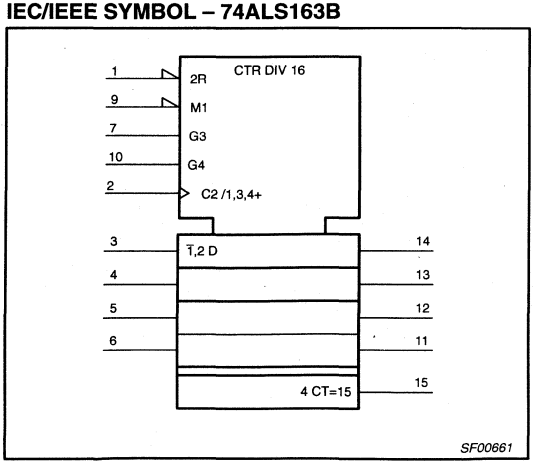
LOGIC SYMBOL – 74ALS163B



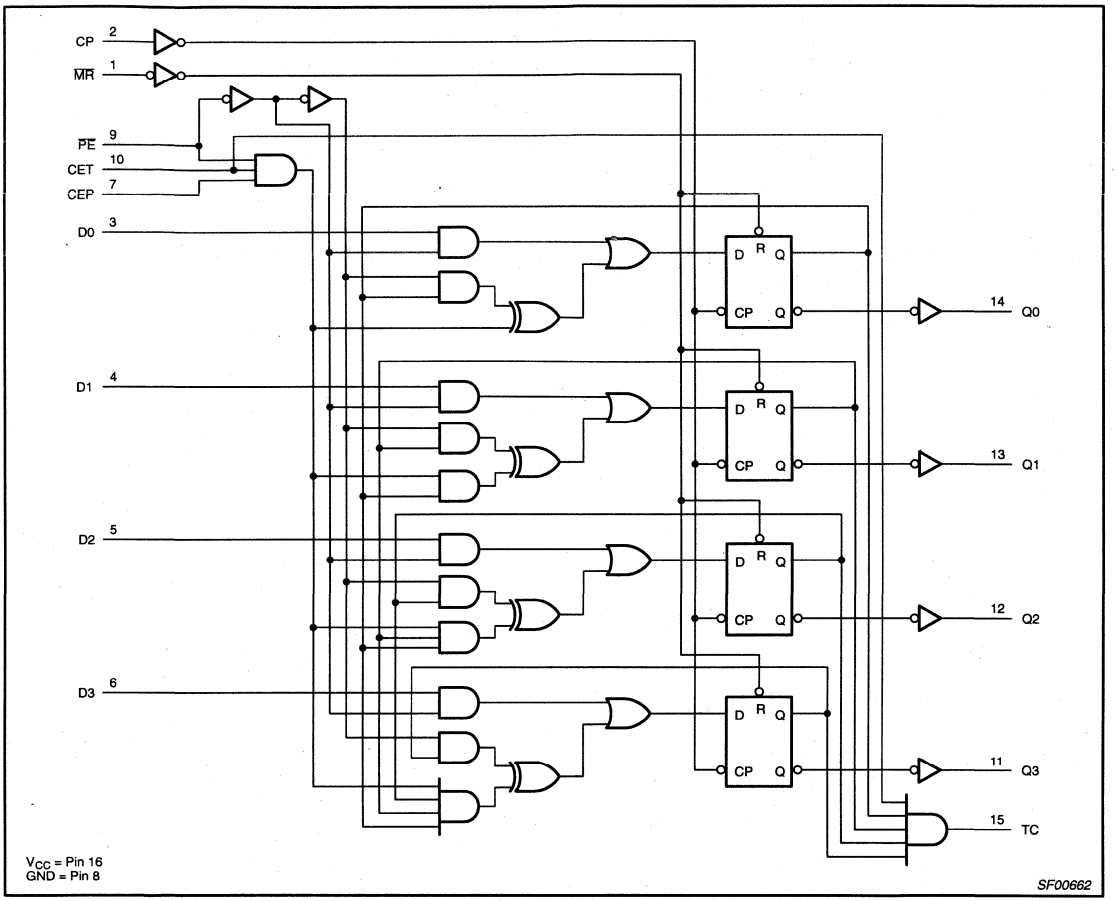
IEC/IEEE SYMBOL – 74ALS161B



IEC/IEEE SYMBOL – 74ALS163B



LOGIC DIAGRAM – 74ALS161B

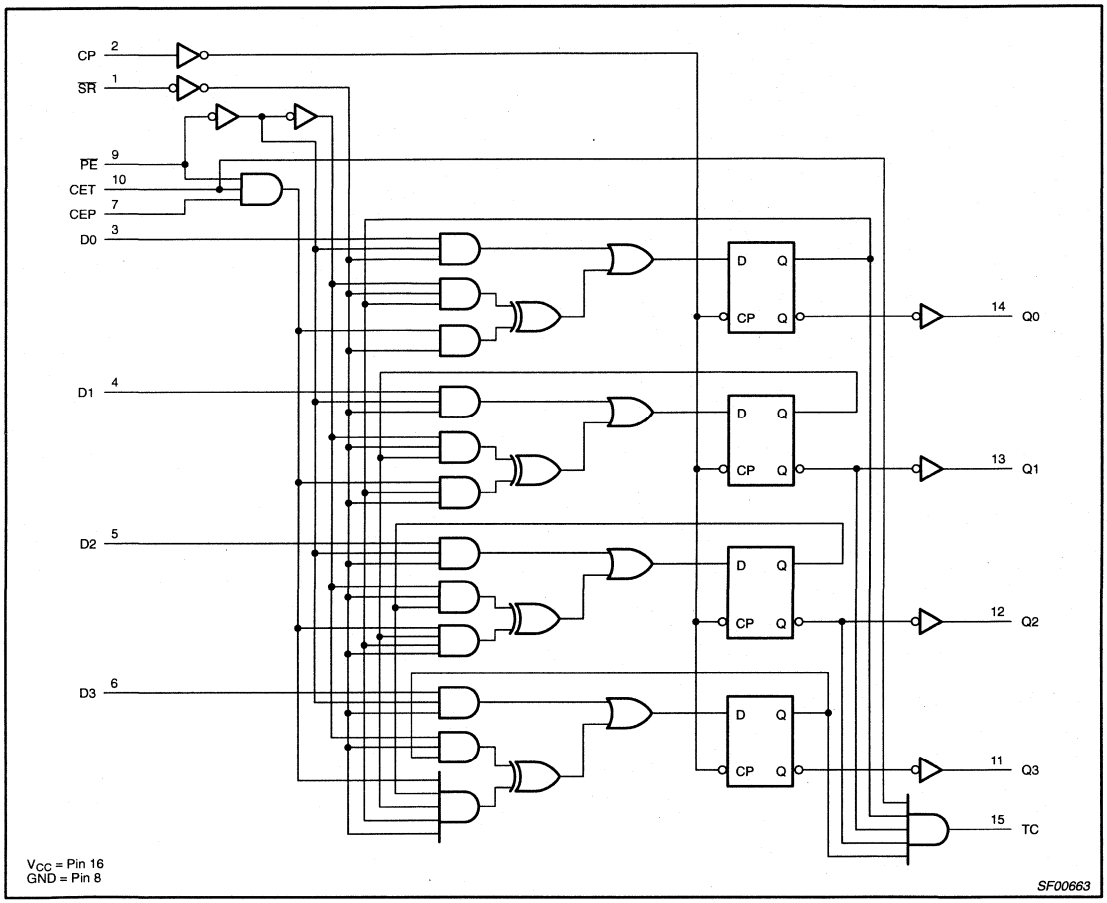


MODE SELECTION FUNCTION TABLE – 74ALS161B

INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(a)	
H	↑	h	h	h	X	count	(a)	Count
h	X	l	X	h	X	qn	(a)	Hold (do nothing)
h	X	X	l	h	X	qn	L	

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
qn = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
(a) = The output is High when CET is High and the counter is at terminal count (HHHH)
↑ = Low-to-High clock transition

LOGIC DIAGRAM – 74ALS163B



MODE SELECTION FUNCTION TABLE – 74ALS163B

INPUTS						OUTPUTS		OPERATING MODE
$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(a)	
h	↑	h	h	h	X	count	(a)	Count
h	X	l	X	h	X	qn	(a)	Hold (do nothing)
h	X	X	l	h	X	qn	L	

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
qn = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
(a) = The output is High when CET is High and the counter is at terminal count (HHHH)
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at minimum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				−0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			10	21	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

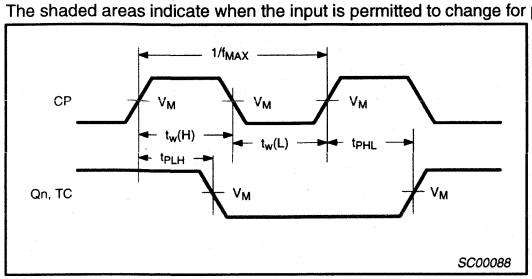
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
f_{MAX}	Maximum clock frequency		Waveform 1	100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	4.0 6.0	13.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	6.0 8.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	3.0 3.0	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	74ALS161B	Waveform 3	8.0	15.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	74ALS163B	Waveform 3	11.0	19.0	ns

AC ELECTRICAL CHARACTERISTICS

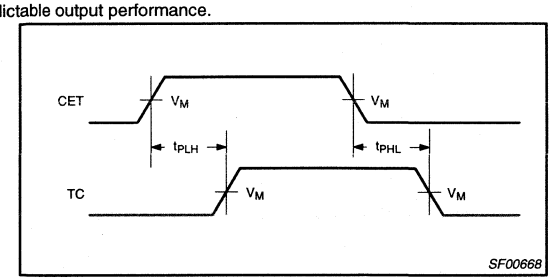
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	Waveform 6	8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 6	0.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 6	0.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low CET or CEP to CP	Waveform 4	10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CET or CEP to CP	Waveform 4	0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width (load), High or Low	Waveform 1	5.0 5.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width (count), High or Low	Waveform 1	5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ or $\overline{SR}$ Pulse width, Low	Waveform 3	5.0		ns
t_{REC}	Recovery time, $\overline{CR}$ or $\overline{SR}$ to CP	Waveform 3	10.0		ns

AC WAVEFORMS

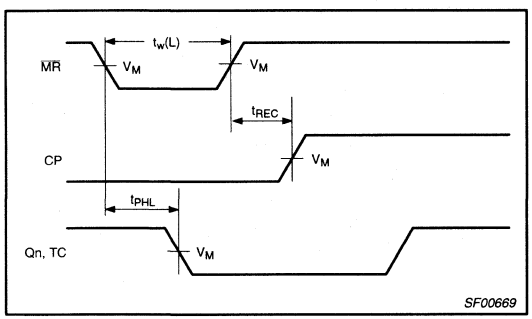
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



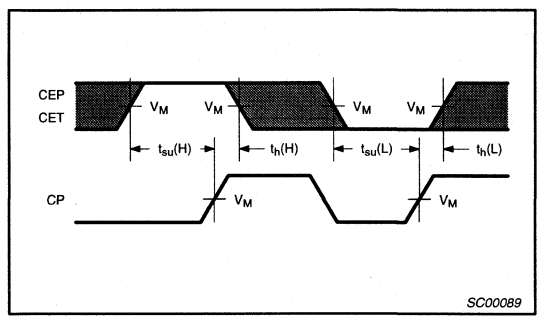
Waveform 1. Propagation Delay for Clock Input to Output, Clock PUlse Width, and Maximum Clock Frequency



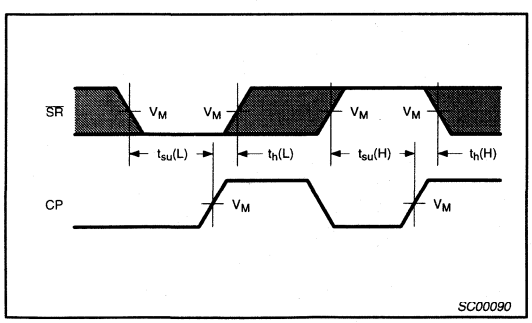
Waveform 2. Propagation Delay for CET to TC Output



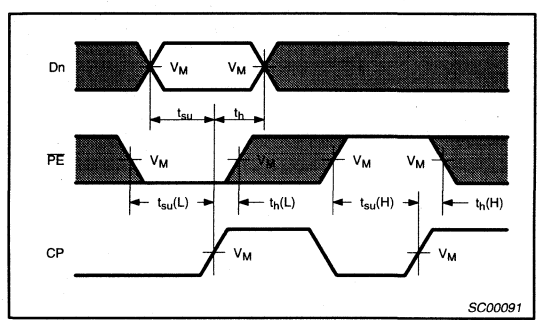
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



Waveform 4. CEP and CET Setup and Hold Times

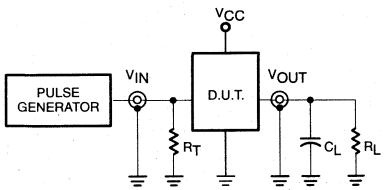


Waveform 5. Synchronous Reset Setup and Hold Times

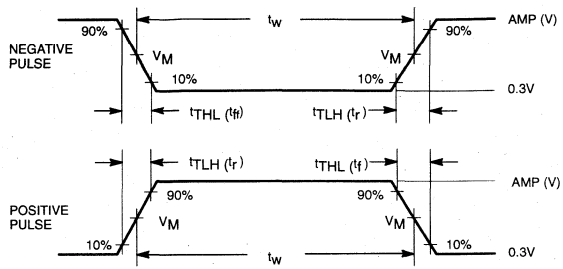


Waveform 6. Data and Parallel Enable Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

8-bit serial-in parallel-out shift register | 74ALS164

FEATURES

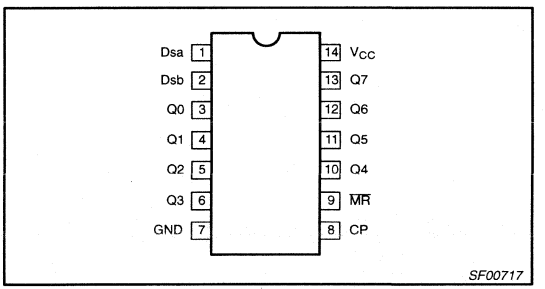
- Gated serial data inputs
- Typical shift frequency of 75MHz
- Asynchronous master reset
- Buffered clock and data inputs
- Fully synchronous data transfer

DESCRIPTION

The 74ALS164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (Dsa, Dsb); either input can be used as an active-high enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-high transition of the clock (CP) input, and enters into Q0 the logical AND of the two data inputs (Dsa, Dsb) that existed one setup time before the rising edge. A Low level on the Master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS164	75MHz	10mA

ORDERING INFORMATION

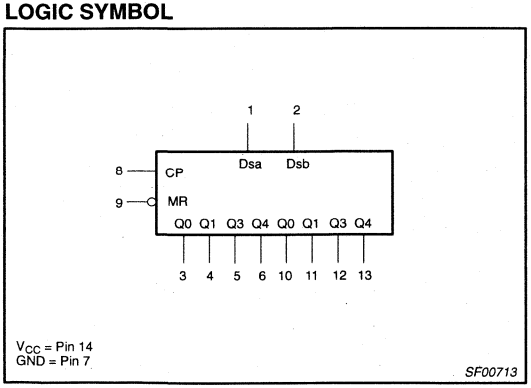
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
14-pin plastic DIP	74ALS164N	SOT27-1
14-pin plastic SO	74ALS164D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

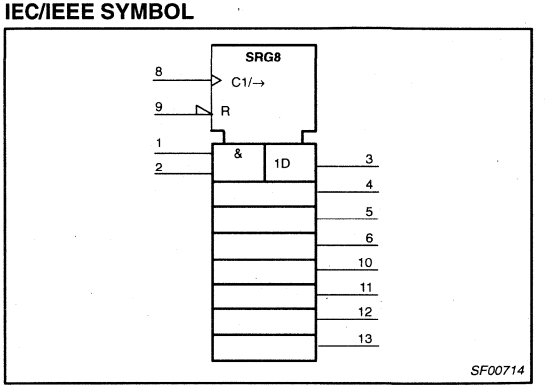
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dsa, Dsb	Data inputs	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q0 – Q7	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

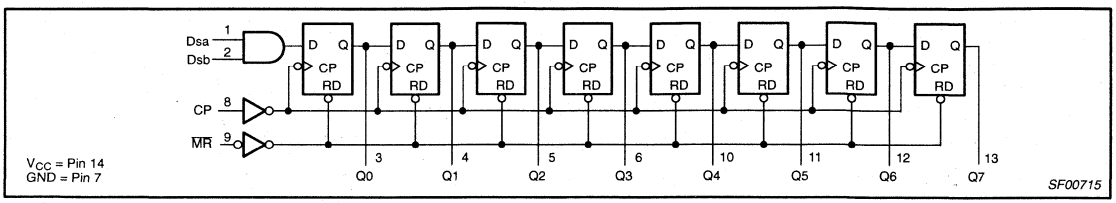
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



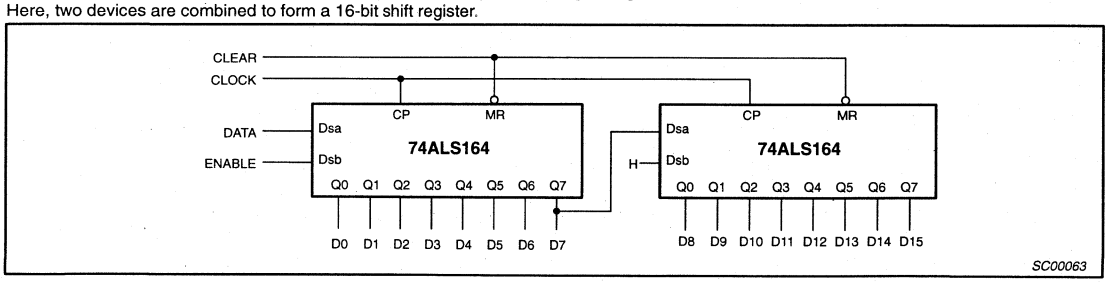
MODE SELECT FUNCTION TABLE

INPUTS				OUTPUTS								OPERATING MODE
$\overline{MR}$	CP	Dsa	Dsb	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	X	X	X	L	L	L	L	L	L	L	L	Reset (Clear)
H	↑	l	l	L	q0	q1	q2	q3	q4	q5	q6	Shift
H	↑	l	h	L	q0	q1	q2	q3	q4	q5	q6	
H	↑	h	l	L	q0	q1	q2	q3	q4	q5	q6	
H	↑	h	h	H	q0	q1	q2	q3	q4	q5	q6	

NOTES:
H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
qn = Lower case letter indicate the state of the referenced output one setup time prior to the Low-to-High clock transition.
X = Don't care
↑ = Low-to-High clock transition

APPLICATION

The 74ALS164 can be cascaded to form synchronous shift registers of longer length.
Here, two devices are combined to form a 16-bit shift register.



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC} − 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			10	15	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	5.0 6.0	13.0 15.0	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Qn	Waveform 2	8.0	18.0	ns

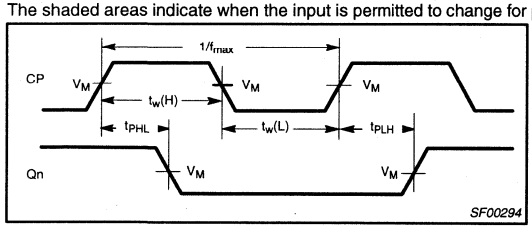
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	Waveform 3	6.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 3	0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	10.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	6.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	6.0		ns

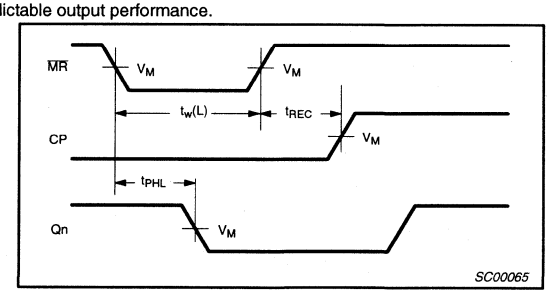
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

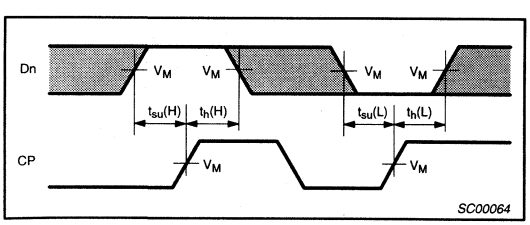
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

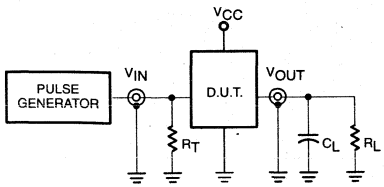


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

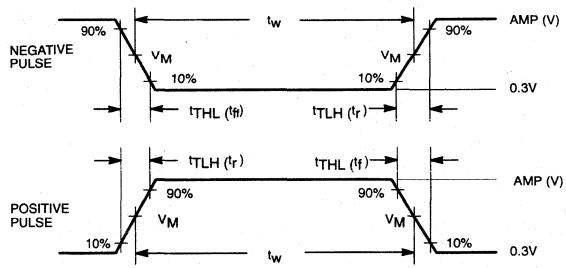


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Hex D flip-flop | 74ALS174

FEATURES

- Four edge-triggered D flip-flops
- Buffered common clock
- Buffered asynchronous master reset

DESCRIPTION

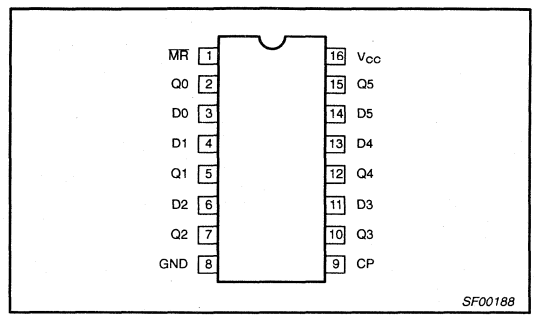
The 74ALS174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of clock or data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the clock and master reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS174	70MHz	7mA

PIN CONFIGURATION



ORDERING INFORMATION

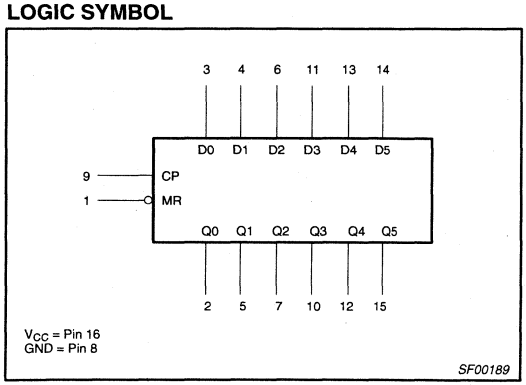
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS174N	SOT38-4
16-pin plastic SO	74ALS174D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

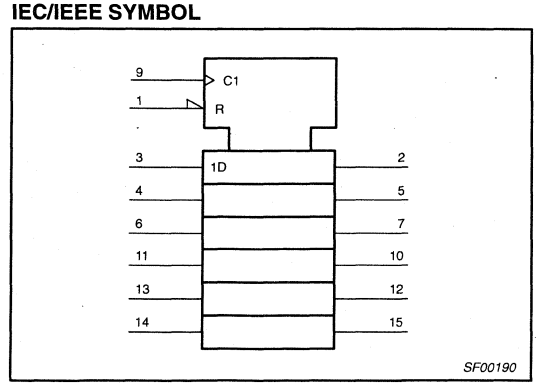
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q0 – Q5	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

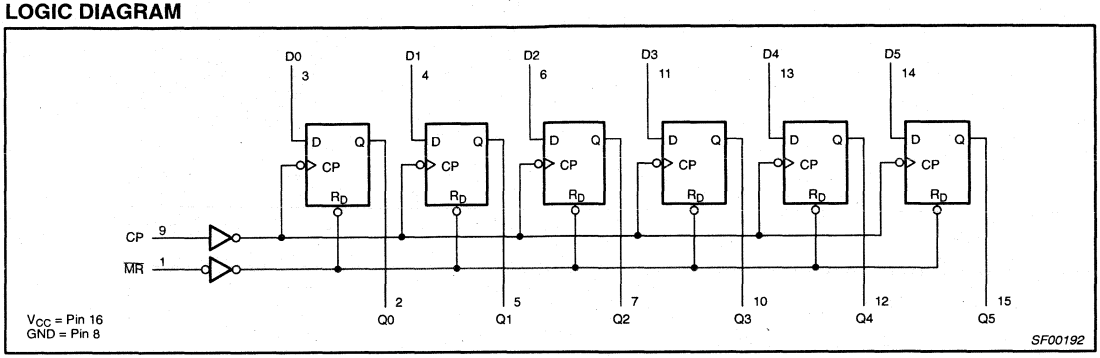
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D	Q_n	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

NOTES:
H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC} – 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			7	14	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

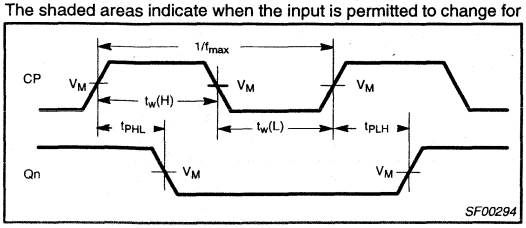
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	5.0 5.0	15.0 15.0	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Qn	Waveform 2	8.0	18.0	ns

AC SETUP REQUIREMENTS

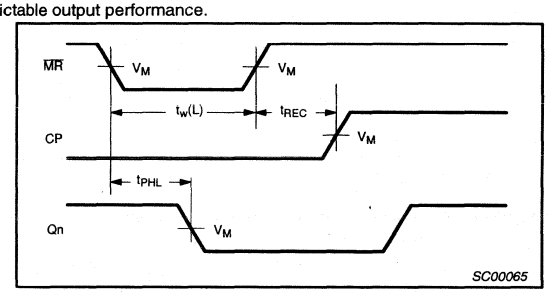
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su}(H) t_{su}(L)	Setup time, High or Low Dn to CP	Waveform 3	6.0 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0		ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 1	8.0 8.0		ns
t_w(L)	$\overline{MR}$ pulse width, Low	Waveform 2	6.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	6.0		ns

AC WAVEFORMS

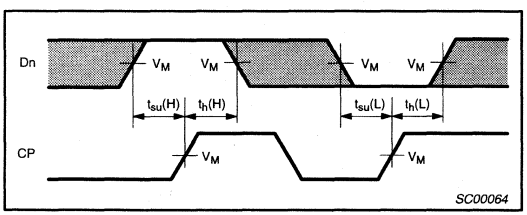
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

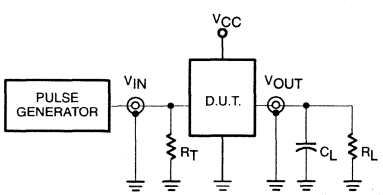


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

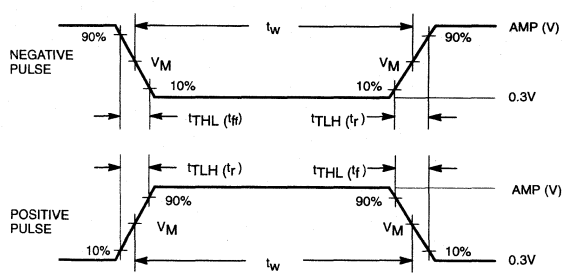


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00005

Quad D flip-flop | 74ALS175

FEATURES

- Four edge-triggered D flip-flops
- Buffered common clock
- Buffered asynchronous master reset
- True and complementary outputs

DESCRIPTION

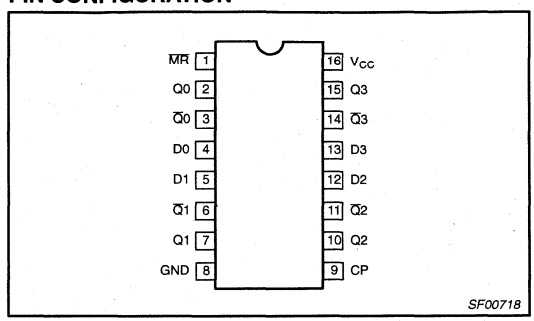
The 74ALS175 is a quad, edge-triggered D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of clock or data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the clock and master reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS175	70MHz	7mA

PIN CONFIGURATION



ORDERING INFORMATION

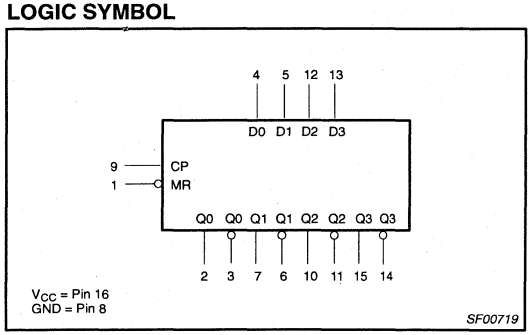
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS175N	SOT38-4
16-pin plastic SO	74ALS175D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

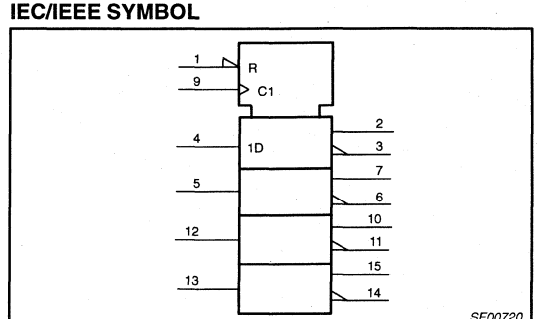
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q0 – Q3	True outputs	20/80	0.4mA/8mA
$\overline{Q}$0 – $\overline{Q}$3	Complementary outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

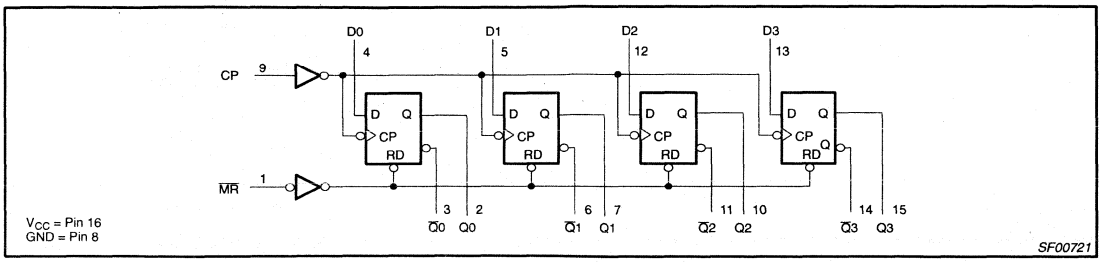
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	D	Q_n	$\overline{Q}_n$	
L	X	X	L	H	Reset (clear)
H	↑	h	H	L	Load "1"
H	↑	l	L	H	Load "0"

NOTES:
H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC} – 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			7	14	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

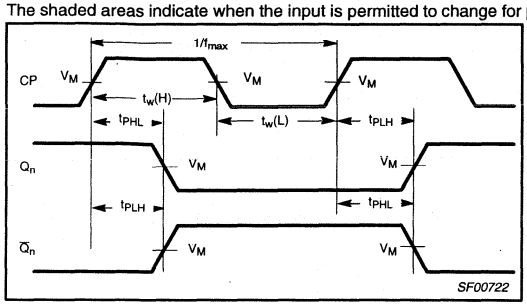
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or CP to $\overline{Qn}$	Waveform 1	3.0 5.0	13.0 16.0	ns
t_{PLH}	Propagation delay, $\overline{MR}$ to Qn	Waveform 2	3.0	13.0	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to $\overline{Qn}$	Waveform 2	8.0	18.0	ns

AC SETUP REQUIREMENTS

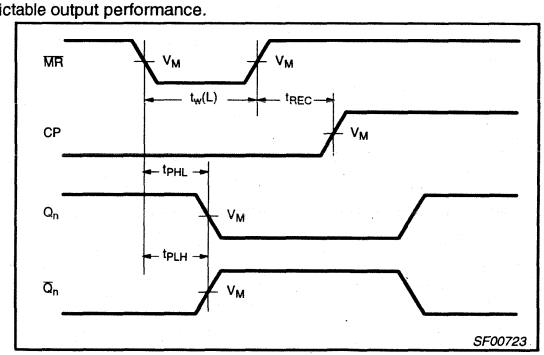
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	8.0 8.0		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	6.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	6.0		ns

AC WAVEFORMS

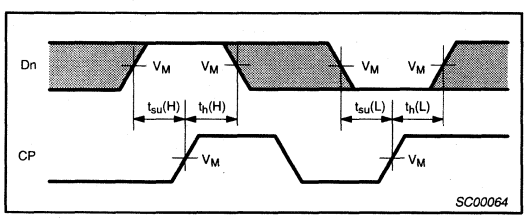
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

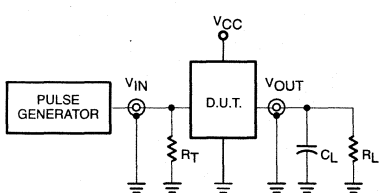


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

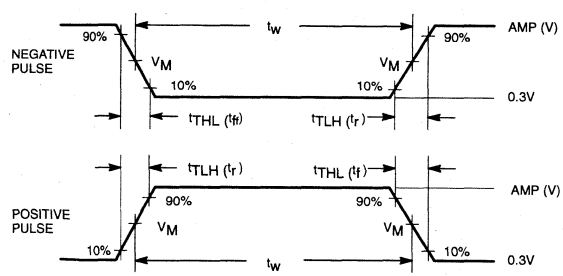


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Octal inverter buffer (3-State)

74ALS240A/ 74ALS240A-1

FEATURES

- Octal bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48 mA

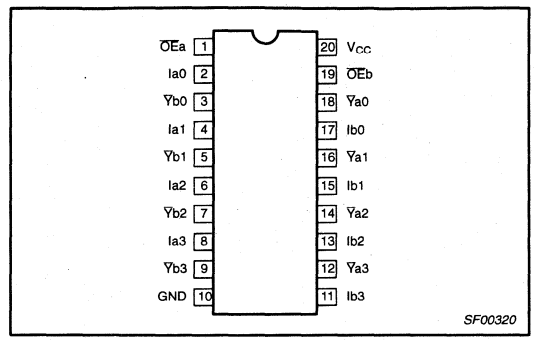
DESCRIPTION

The 74ALS240A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3-State outputs.

The 74ALS240A-1 sinks 48 mA I_{OL} if the V_{CC} is limited to 5.0V ±0.25V.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS240A	4.5ns	15mA
74ALS240A-1	4.5ns	15mA

PIN CONFIGURATION



ORDERING INFORMATION

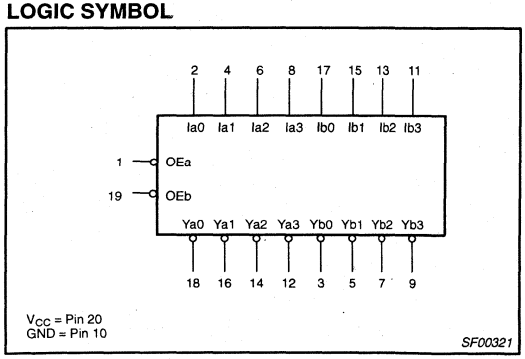
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS240AN, 74ALS240A-1N	SOT146-1
20-pin plastic SOL	74ALS240AD, 74ALS240A-1D	SOT163-1
20-pin plastic SSOP Type II	74ALS240ADB, 74ALS240A-1DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

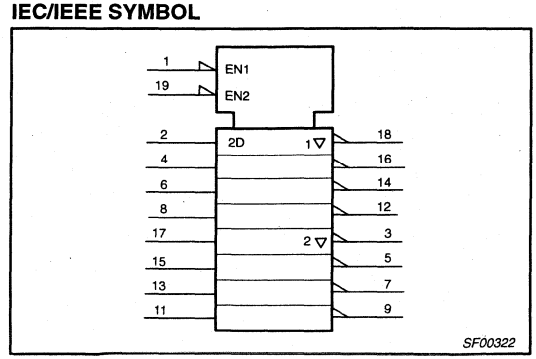
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}a$, $\overline{OE}b$	Output Enable inputs (active-Low)	1.0/1.0	20µA/0.1mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs	750/240	15mA/24mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



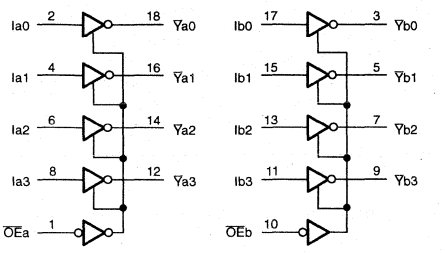
IEC/IEEE SYMBOL



Octal inverter buffer (3-State)

74ALS240A/ 74ALS240A-1

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

SF00323

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48 [1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –3mA	2.4	3.2		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
		-1 version	V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			2.5	11	mA
		I_{CCL}				19.5	23	mA
		I_{CCZ}				23	30	

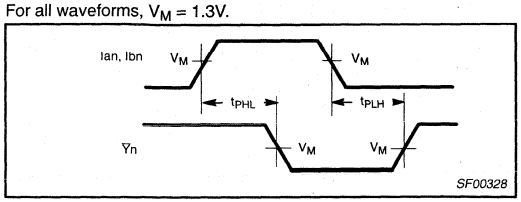
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

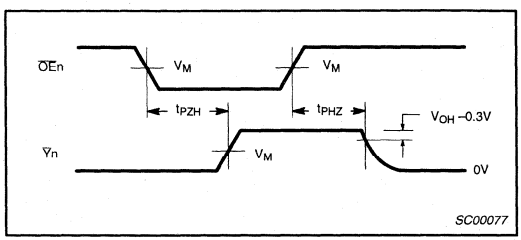
SYMBOL	PARAMETER	TEST CONDITION	LIMITS (T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω) MIN	LIMITS MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 3.0	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 3.0	10.0 12.0	ns

AC WAVEFORMS

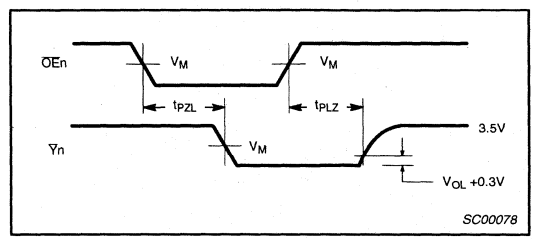
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Non-Inverting Output

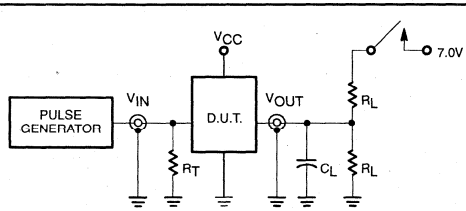


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

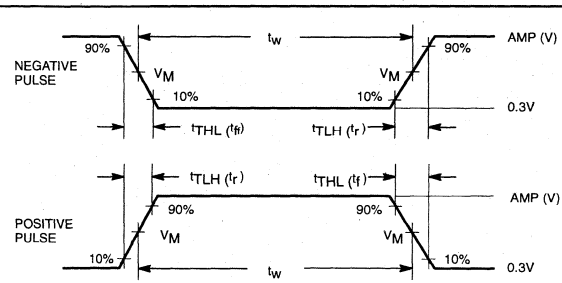
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Octal buffer (3-State) — 74ALS241A/74ALS241A-1

FEATURES

- Octal bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48 mA

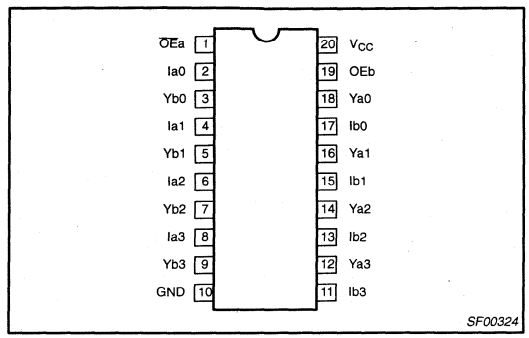
DESCRIPTION

The 74ALS241A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}a$ and OEb, each controlling four of the 3-State outputs.

The 74ALS241A-1 sinks 48mA I_{OL} if the V_{CC} is limited to 5.0V ±0.25V.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS241A	4.5ns	18mA
74ALS241A-1	4.5ns	18mA

PIN CONFIGURATION



ORDERING INFORMATION

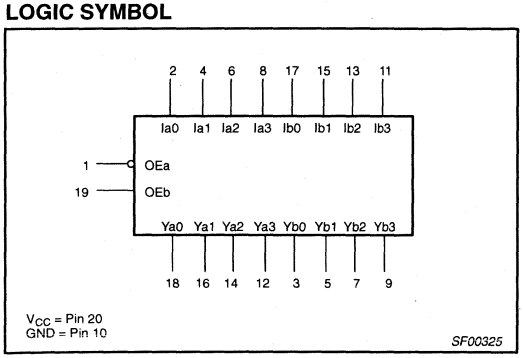
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS241AN, 74ALS241A-1N	SOT146-1
20-pin plastic SOL	74ALS241AD, 74ALS241A-1D	SOT163-1
20-pin plastic SSOP Type II	74ALS241ADB, 74ALS241A-1DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

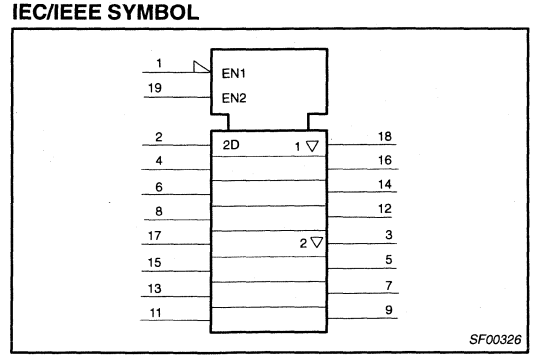
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}a$, $\overline{OE}b$	Output Enable inputs (active-Low)	1.0/1.0	20µA/0.1mA
Yan, Ybn	Data outputs	750/240	15mA/24mA
Yan, Ybn	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

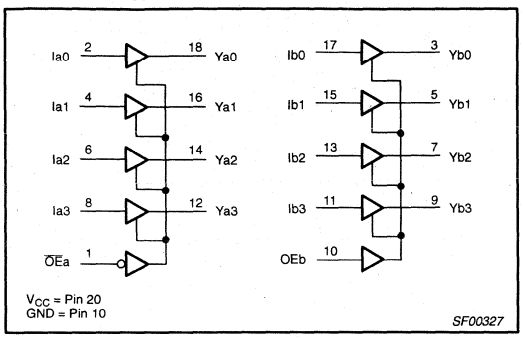
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48 [1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –3mA	2.4	3.2		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
		-1 version	V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			7	15	mA
		I_{CCL}				21	26	mA
		I_{CCZ}				25	30	mA

NOTES:

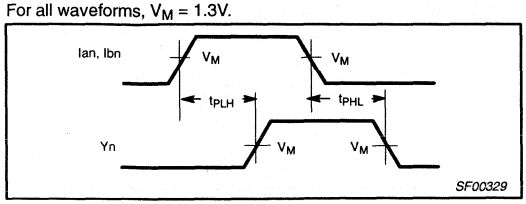
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

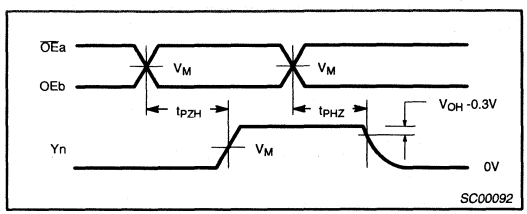
SYMBOL	PARAMETER	TEST CONDITION	LIMITS (T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω) MIN	LIMITS MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	1.5 1.5	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	1.0 2.5	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	1.0 2.5	10.0 12.0	ns

AC WAVEFORMS

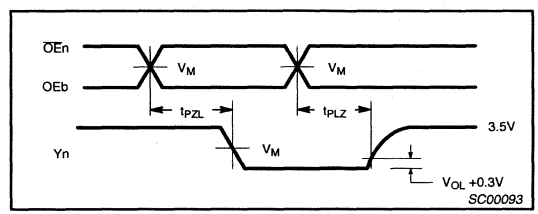
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Non-Inverting Output

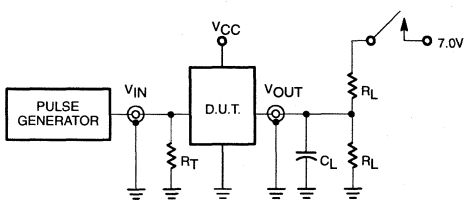


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

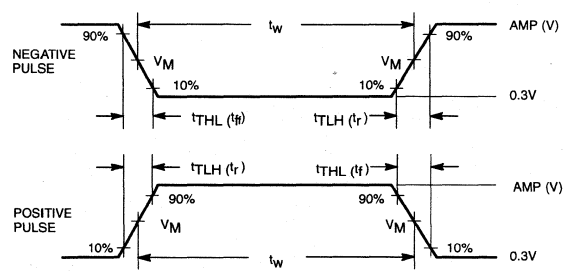
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Octal buffer (3-State) | 74ALS244A/74ALS244A-1

FEATURES

- Octal bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48mA

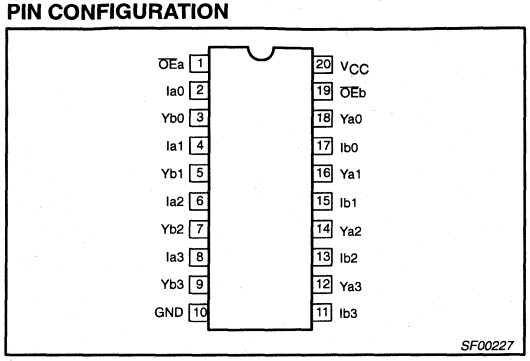
DESCRIPTION

The 74ALS244A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3-State outputs.

The 74ALS244A-1 sinks 48 mA I_{OL} if the V_{CC} is limited to 5.0V ±0.25V.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS244A	4.5ns	17mA
74ALS244A-1	4.5ns	17mA

PIN CONFIGURATION



ORDERING INFORMATION

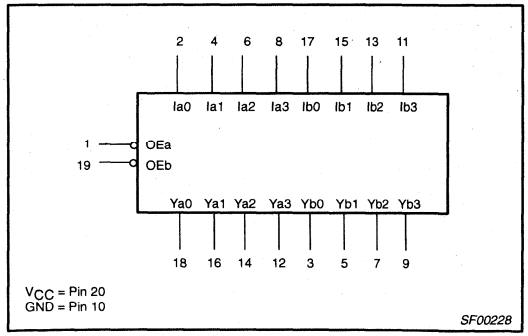
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS244AN, 74ALS244A-1N	SOT146-1
20-pin plastic SOL	74ALS244AD, 744ALS244A-1D	SOT163-1
20-pin plastic SSOP Type II	74ALS244ADB, 74ALS244A-1DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

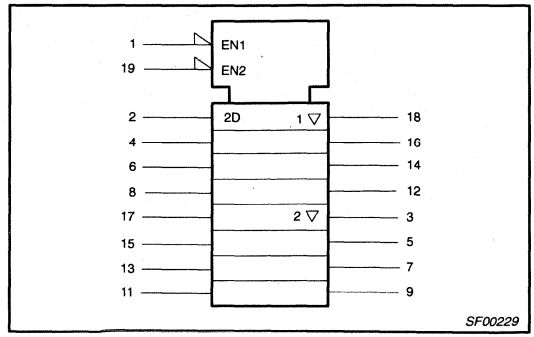
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}a$, $\overline{OE}b$	Output Enable inputs (active-Low)	1.0/1.0	20µA/0.1mA
Yan, Ybn	Data outputs	750/240	15mA/24mA
Yan, Ybn	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

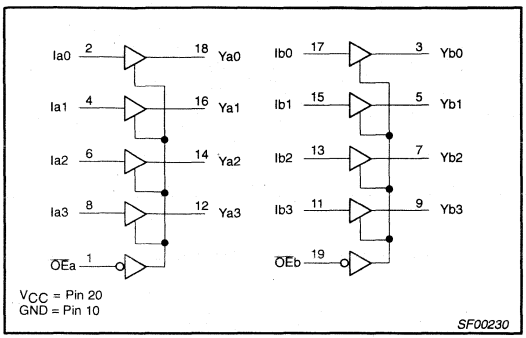
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 versions			48[1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTES:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –3mA	2.4	3.2		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
		-1 version	V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			6.5	15	mA
		I_{CCL}				19.5	24	mA
		I_{CCZ}				25	30	mA

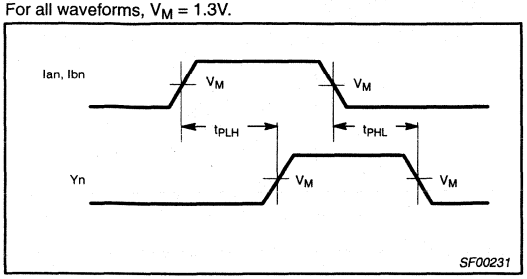
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

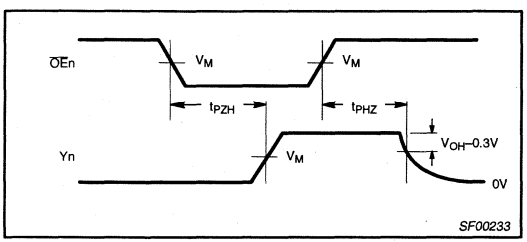
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	1.5 1.5	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	1.0 2.5	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.5	10.0 12.0	ns

AC WAVEFORMS

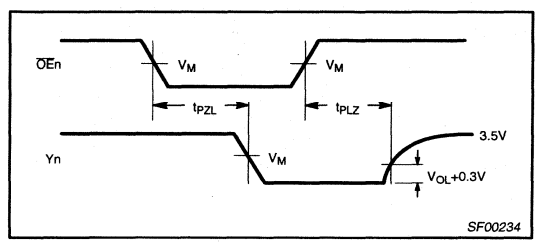
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Non-inverting Outputs

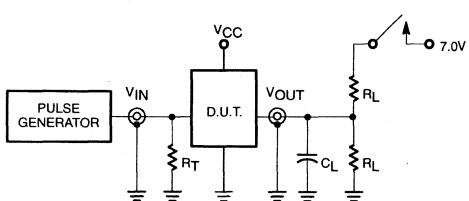


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

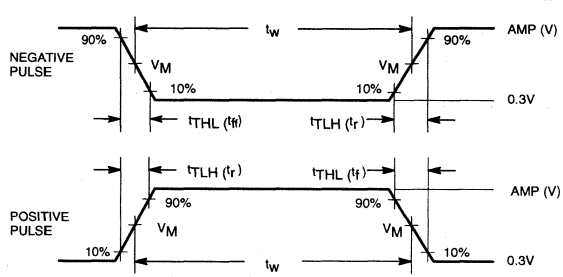
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Octal transceiver (3-State) 74ALS245A/74ALS245A-1

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- Outputs are placed in high impedance state during power-off conditions
- The -1 version sinks 48mA

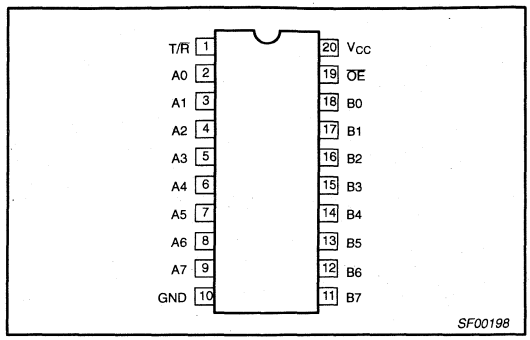
DESCRIPTION

The 74ALS245A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The device features an output enable ($\overline{OE}$) input for easy cascading and transmit/receive (R/$\overline{T}$) input for direction control.

The 74ALS245A-1 is the same as the 74ALS245A except that both ports sink 48mA within the ±5% V_{CC} range.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS245A	7.0ns	34mA
74ALS245A-1	7.0ns	34mA

PIN CONFIGURATION



ORDERING INFORMATION

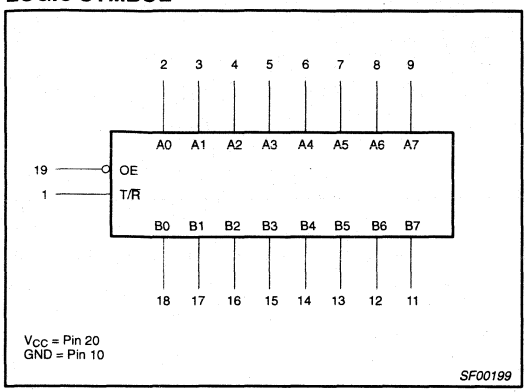
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS245AN, 74ALS245A-1N	SOT146-1
20-pin plastic SOL	74ALS245AD, 744ALS245A-1D	SOT163-1
20-pin plastic SSOP Type II	74ALS245ADB, 74ALS245A-1DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

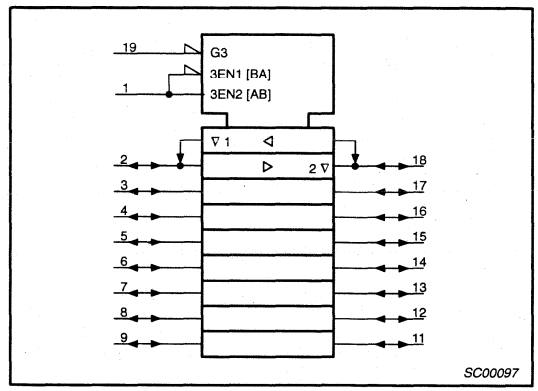
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20µA/0.1mA
T/$\overline{R}$	Transmit/receive input	1.0/1.0	20µA/0.1mA
A0 – A7	A port outputs	750/240	15mA/24mA
B0 – B7	B port outputs	750/240	15mA/24mA
A0 – A7	A port outputs (-1 version)	750/480	15mA/48mA
B0 – B7	B port outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

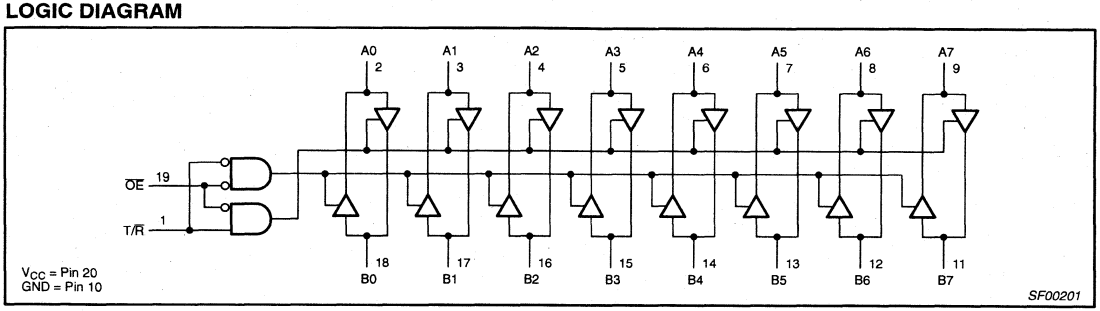
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48[1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTES:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –3mA	2.4	3.2		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
		-1 version	V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	$\overline{OE}$ or T/$\overline{R}$	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		A or B ports	V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current[3]		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current[3]		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_O	Output current[4]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			28	45	mA
		I_{CCL}				40	55	mA
		I_{CCZ}				44	58	mA

NOTES:

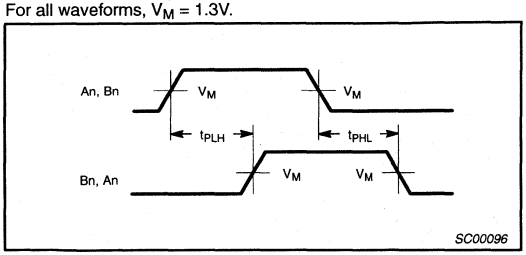
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

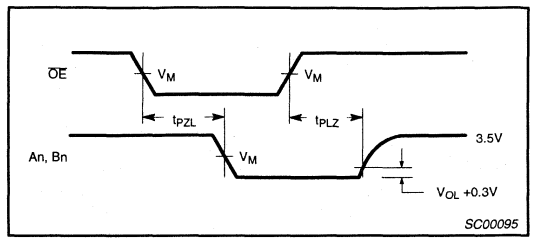
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	LIMITS MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	20.0 20.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 4.0	10.0 15.0	ns

AC WAVEFORMS

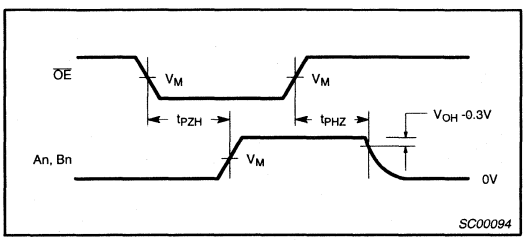
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Non-inverting Outputs

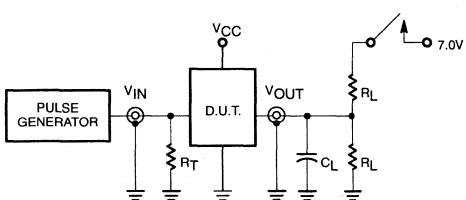


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

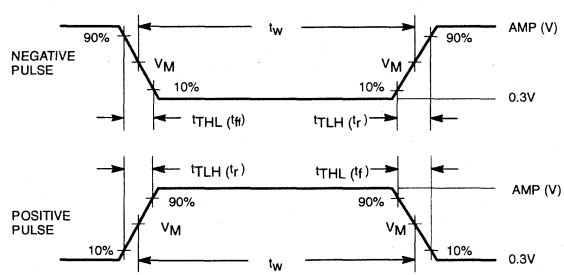
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

8-input multiplexer (3-State) 74ALS251

FEATURES

- 8-to-1 multiplexing
- On chip decoding
- Multifunction capability
- Inverting and non-inverting outputs
- Both outputs are 3-State for further multiplexer expansion

DESCRIPTION

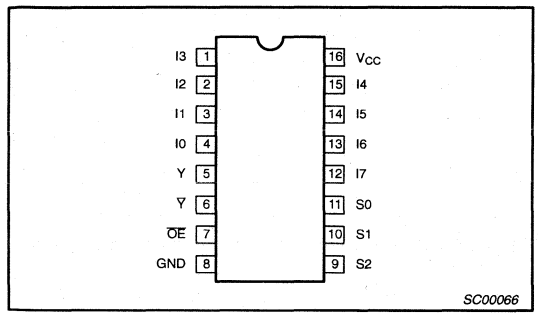
The 74ALS251 is a logic implementation of a single 8-position switch with the switch position controlled by the state of three select (S0, S1, S2) inputs. True (Y) and complementary ($\overline{Y}$) outputs are both provided.

The output enable ($\overline{OE}$) is active Low. When $\overline{OE}$ is High, both outputs are in High impedance state, allowing multiple connections to a common bus without driving nor loading the bus significantly.

When the outputs of more than one device are tied together, the user must ensure that there is no overlap in the active-Low portion of the output enable voltages in order to avoid high currents that could exceed the maximum current rating.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS251	7.0ns	7.5mA

PIN CONFIGURATION



ORDERING INFORMATION

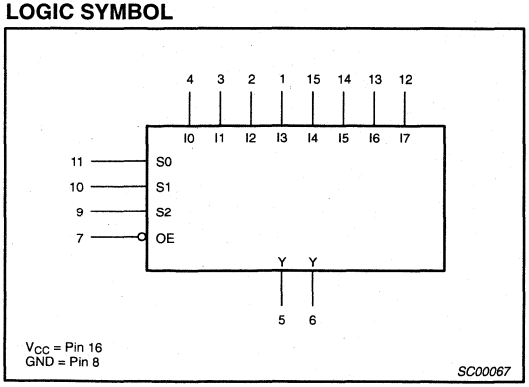
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS251N	SOT38-4
16-pin plastic SO	74ALS251D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

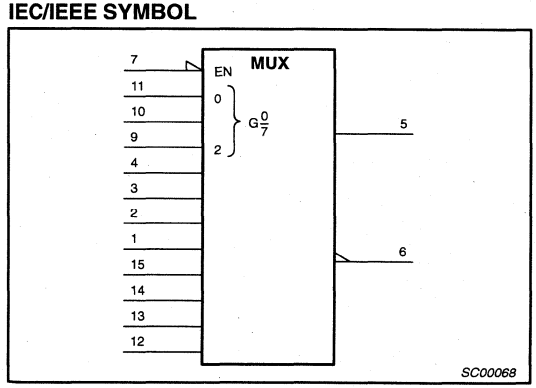
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0 – I7	Data inputs	1.0/1.0	20µA/0.1mA
S0 – S2	Select inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20µA/0.1mA
Y, $\overline{Y}$	Data outputs	130/240	2.5mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

LOGIC SYMBOL

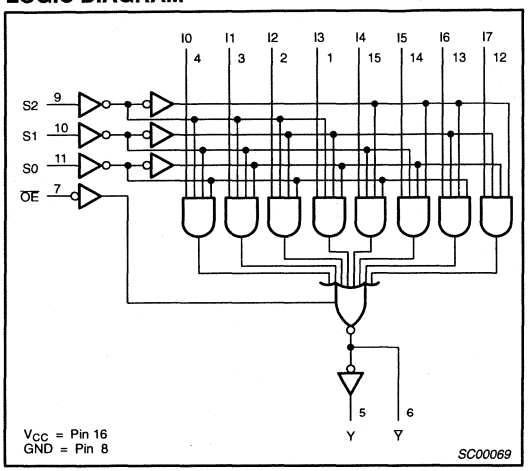


IEC/IEEE SYMBOL



8-input multiplexer (3-State) 74ALS251

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S2	S1	S0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –2.6mA	2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CC}	V_{CC} = MAX			7.0	10	mA
		I_{CCZ}				9.0	14	mA

NOTES:

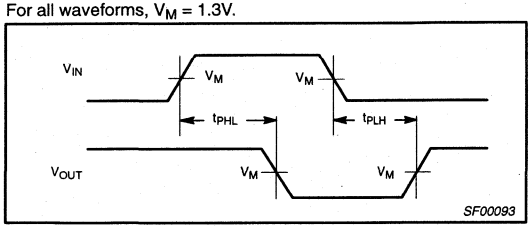
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

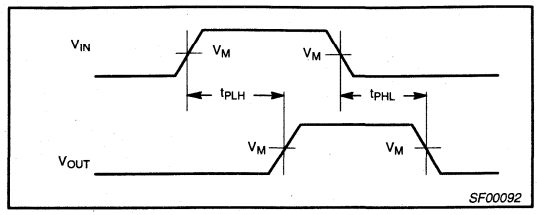
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Y	Waveform 2	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay In to $\overline{Y}$	Waveform 1	3.0 6.0	10.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Y	Waveform 1, 2	5.0 7.0	15.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to $\overline{Y}$	Waveform 1, 2	8.0 5.0	17.0 15.0	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	Waveform 3 Waveform 4	2.0 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	Waveform 3 Waveform 4	2.0 1.0	8.0 7.0	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	Waveform 3 Waveform 4	2.0 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	Waveform 3 Waveform 4	2.0 1.0	8.0 7.0	ns

AC WAVEFORMS

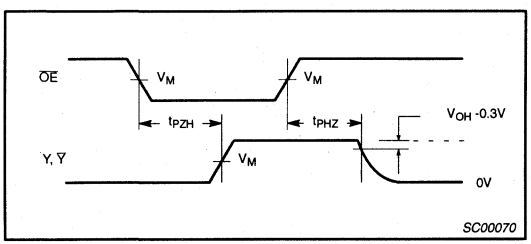
For all waveforms, V_M = 1.3V.



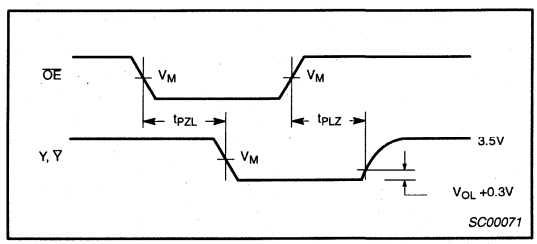
Waveform 1. Propagation Delay for Inverting Output



Waveform 2. Propagation Delay for Non-inverting Output

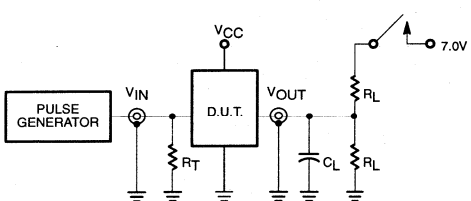


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

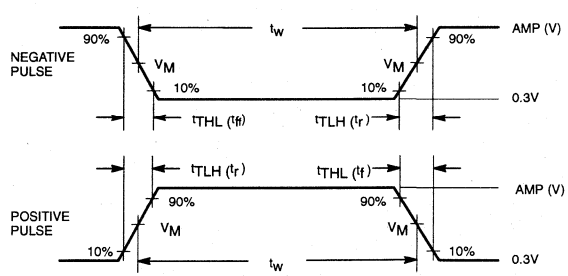
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Dual 4-input multiplexer (3-State) 74ALS253

FEATURES

- 3-State outputs for bus interface and multiplex operation
- Common select inputs
- Separate output enable inputs

DESCRIPTION

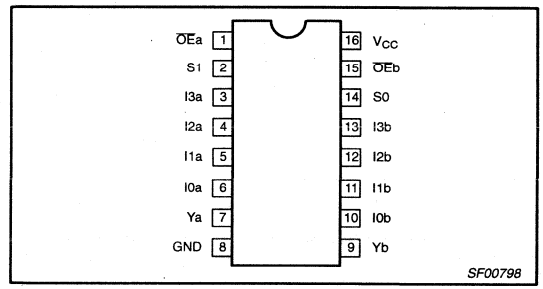
The 74ALS253 has two identical 4-input multiplexers with 3-State outputs which select 2 bits from four sources by using common select input (S0, S1). When the individual output enable ($\overline{OE}$a, $\overline{OE}$b) inputs of the 4-input multiplexers are High, the outputs are forced to a High impedance (Z) state.

The 74ALS253 is the logic implementation of 2-pole, 4-position switch being determined by the logic levels supplied to the common select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-State devices are tied together, all but one device must be in the High impedance state. Therefore, only one output enable must be achieved at a time.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS253	7.0ns	8mA

PIN CONFIGURATION



ORDERING INFORMATION

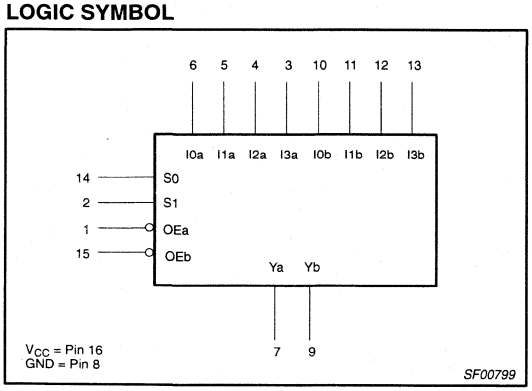
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	74ALS253N	SOT38-4
16-pin plastic SO	74ALS253D	SOT109-1
16-pin plastic SSOP Type II	74ALS253DB	SOT338-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

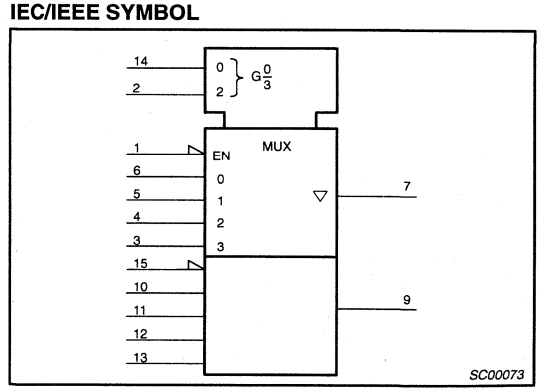
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a – I3a	Port A data inputs	1.0/1.0	20µA/0.1mA
I0b – I3b	Port B data inputs	1.0/1.0	20µA/0.1mA
S0, S1	Common select inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}$a	Port A Output Enable input (active-Low)	1.0/1.0	20µA/0.1mA
$\overline{OE}$b	Port B Output Enable input (active-Low)	1.0/1.0	20µA/0.1mA
Ya – Yb	3-State outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

LOGIC SYMBOL

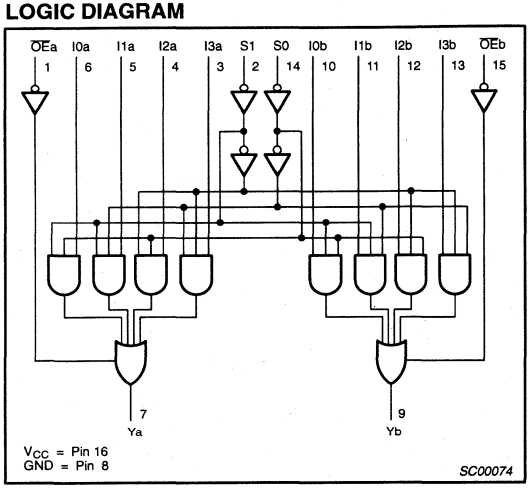


IEC/IEEE SYMBOL



Dual 4-input multiplexer (3-State) 74ALS253

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS
S0	S1	I0	I1	I2	I3	$\overline{OE}$n	Yn
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –2.6mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CC}	V_{CC} = MAX			7.0	12	mA
		I_{CCZ}				9.0	14	mA

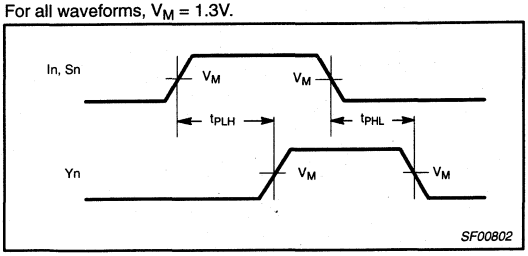
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

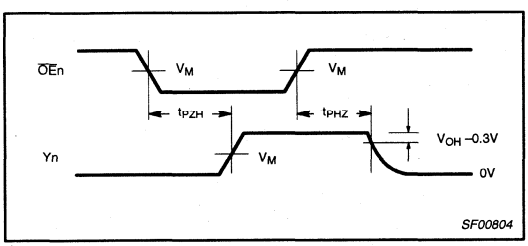
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Yn	Waveform 1	5.0 7.0	15.0 16.0	ns
t_{PZH} t_{PZL}	Output enable time, High or Low level $\overline{OE}$n to Yn	Waveform 2 Waveform 3	1.0 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time, High or Low level $\overline{OE}$n to Yn	Waveform 2 Waveform 3	1.0 1.0	7.0 7.0	ns

AC WAVEFORMS

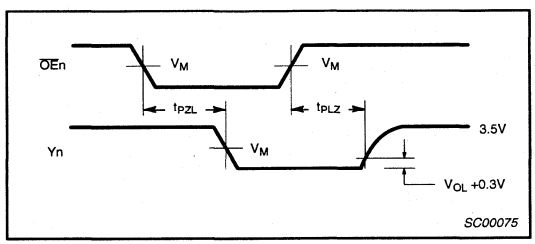
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Data and Select to Output

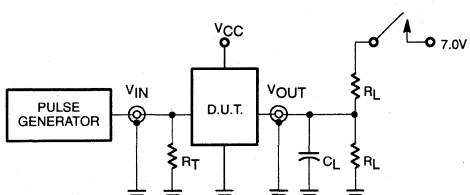


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

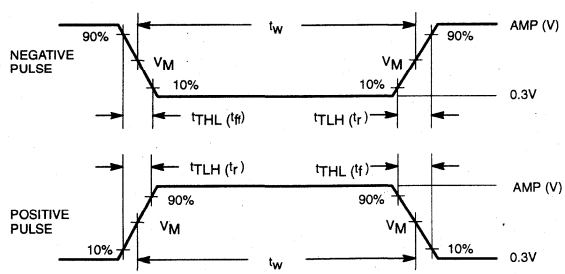
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Data selector/multiplexer 74ALS257/74ALS258

74ALS257 Quad 2-input data selector, non-inverting (3-State)
74ALS258 Quad 2-input data selector, inverting (3-State)

DESCRIPTION

The 74ALS257 is a quad 2-input multiplexer which selects 4 bits of data from one of two sources under the control of a common select input (S). The output enable input ($\overline{OE}$) is active when Low. When $\overline{OE}$ is High, all of the outputs (Yn) are forced to a High impedance state (3-State) regardless of all other input conditions.

Moving data from two registers to a common output bus is a typical use of the 74ALS257. The state of the select input determines the particular register from which data comes.

The device is the logic implementation of 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the select input. The 74ALS258 is similar but has inverting outputs ($\overline{Y}$n).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS257	7.0ns	7mA
74ALS258	7.0ns	7mA

ORDERING INFORMATION

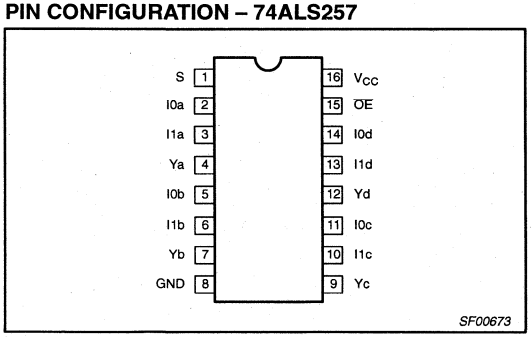
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS257N, 74ALS258	SOT38-4
16-pin plastic SO	74ALS257D, 74ALS258D	SOT109-1
16-pin plastic SSOP Type II	74ALS257DB, 74ALS258DB	SOT338-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

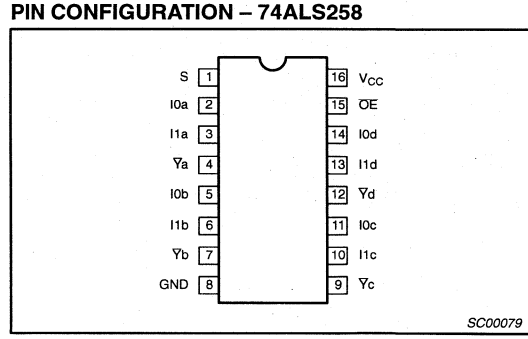
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ina, Inb, Inc, Ind	Data inputs	1.0/1.0	20µA/0.1mA
S	Select input	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Enable input	1.0/1.0	20µA/0.1mA
Ya – Yd, $\overline{Y}$a – $\overline{Y}$d	Data outputs	20/240	0.4mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

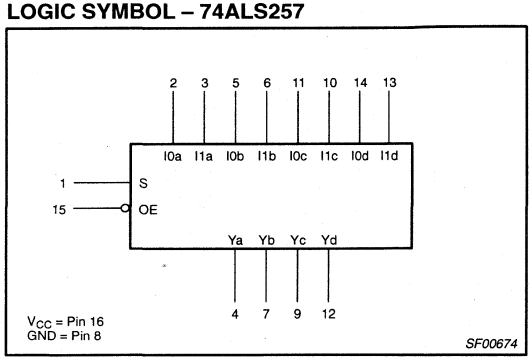
PIN CONFIGURATION – 74ALS257



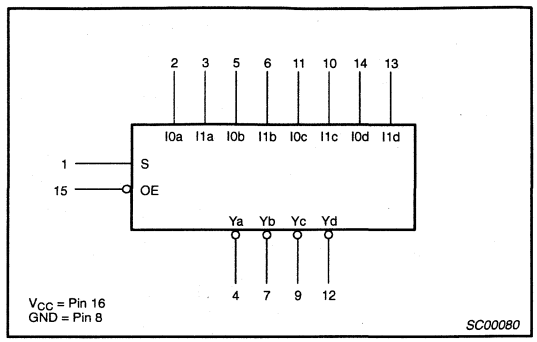
PIN CONFIGURATION – 74ALS258



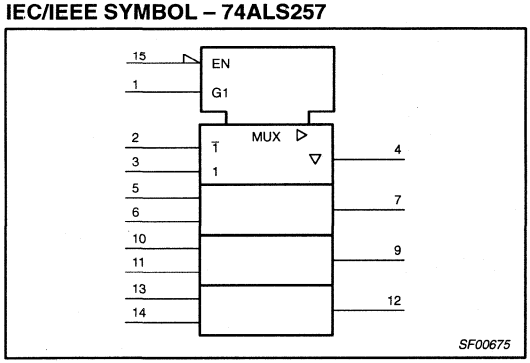
LOGIC SYMBOL – 74ALS257



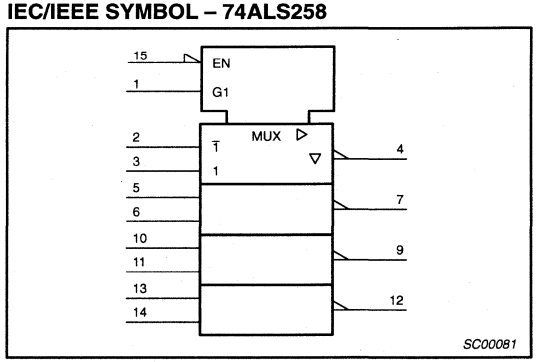
LOGIC SYMBOL – 74ALS258



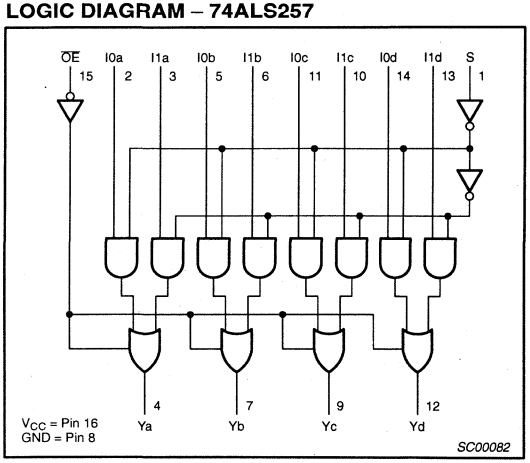
IEC/IEEE SYMBOL – 74ALS257



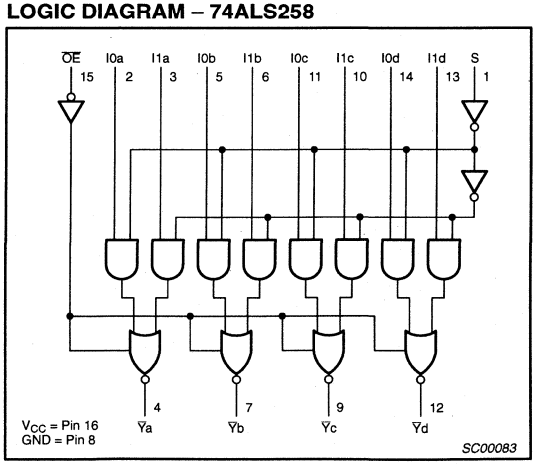
IEC/IEEE SYMBOL – 74ALS258



LOGIC DIAGRAM – 74ALS257



LOGIC DIAGRAM – 74ALS258



FUNCTION TABLE – 74ALS257

INPUTS				OUTPUT
$\overline{OE}$	S	I0n	I1n	Yn
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE – 74ALS258

INPUTS				OUTPUT
$\overline{OE}$	S	I0n	I1n	$\overline{Y}$n
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
					I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	74ALS257	I_{CCH}	V_{CC} = MAX			3	6	mA
			I_{CCL}				8	12	mA
			I_{CCZ}				9	14	mA
		74ALS258	I_{CCH}	V_{CC} = MAX			2.5	4	mA
			I_{CCL}				7	11	mA
			I_{CCZ}				9	13	mA

NOTES:

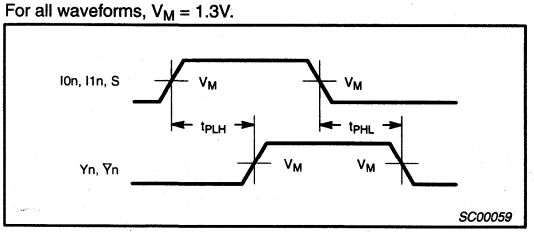
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

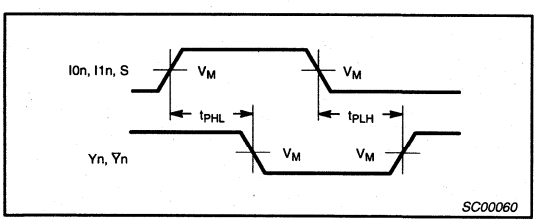
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I0n or I1n to Yn	74ALS257	Waveform 1	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Yn		Waveform 1, 2	4.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to Yn		Waveform 3 Waveform 4	3.0 4.0	11.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to Yn		Waveform 3 Waveform 4	2.0 5.0	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I0n or I1n to $\overline{Y}$n	74ALS258	Waveform 1	2.0 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$n		Waveform 1, 2	4.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to Yn		Waveform 3 Waveform 4	3.0 4.0	11.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to $\overline{Y}$n		Waveform 3 Waveform 4	2.0 5.0	9.0 12.0	ns

AC WAVEFORMS

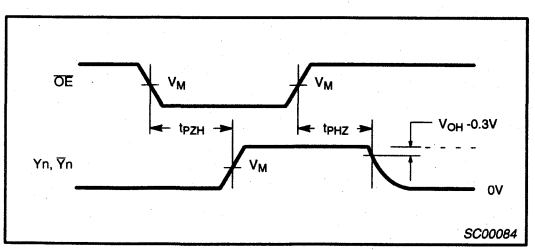
For all waveforms, V_M = 1.3V.



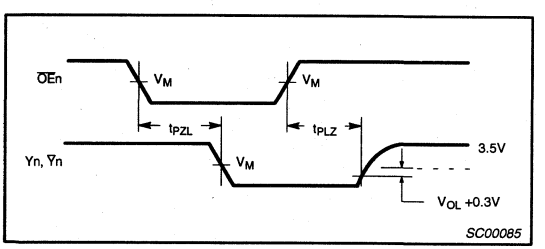
Waveform 1. Propagation Delay for Data and Select to Outputs



Waveform 2. Propagation Delay for Data and Select to Outputs

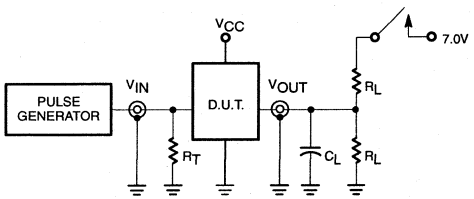


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

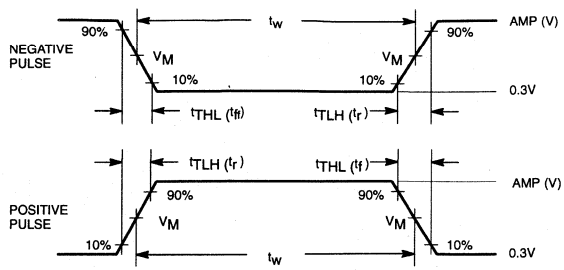
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Octal D-type flip-flop | 74ALS273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous master reset
- See 74ALS377 for clock enable version
- See 74ALS373 for transparent latch version
- See 74ALS374 for 3-State version

DESCRIPTION

The 74ALS273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset all flip-flops simultaneously.

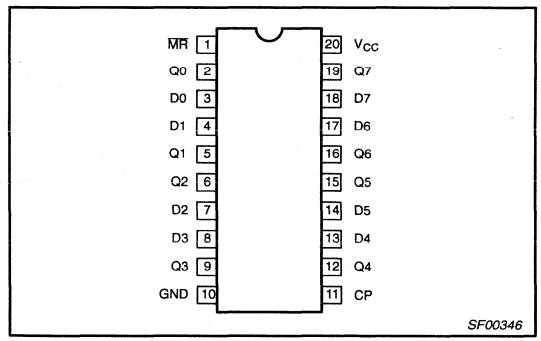
The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of clock or data inputs by a Low voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all flip-flops.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS273	95MHz	16mA

PIN CONFIGURATION



ORDERING INFORMATION

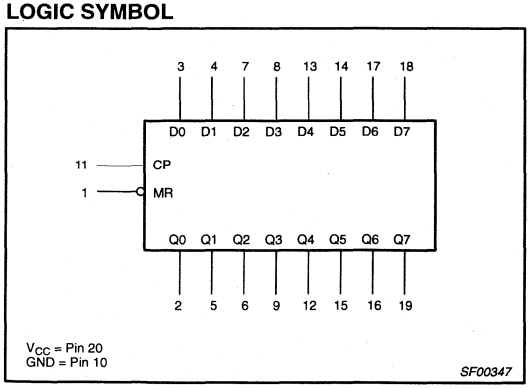
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS273N	SOT146-1
20-pin plastic SO	74ALS273D	SOT163-1
20-pin plastic SSOP Type II	74ALS273DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

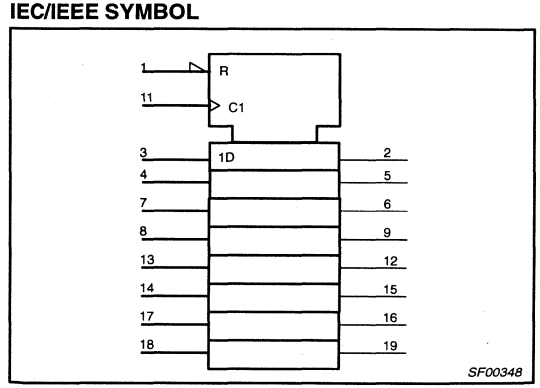
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/2.0	20µA/0.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q0 – Q7	3-State outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

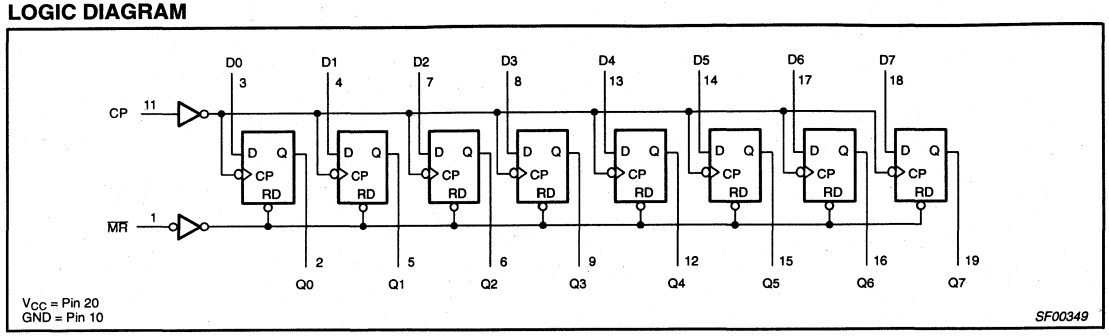
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Qn	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{MR}$, CP	V_{CC} = MAX, V_I = 0.4V				–0.1	mA
		Dn					–0.2	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			12	18	mA
		I_{CCL}				21	29	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

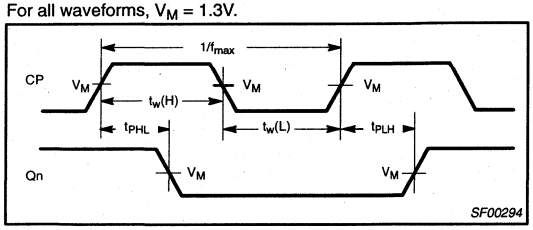
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	65		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.0 3.0	8.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 2	4.0	12.0	ns

AC SETUP REQUIREMENTS

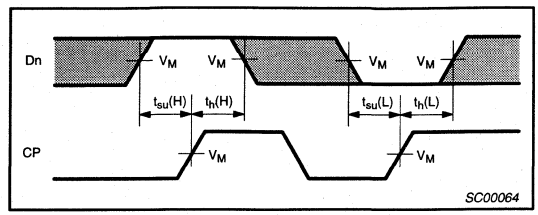
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su}(H) t_{su}(L)	Setup time, High or Low Dn to CP	Waveform 3	5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0		ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 1	6.0 8.0		ns
t_w(L)	$\overline{MR}$ pulse width, Low	Waveform 2	7.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	12.0		ns

AC WAVEFORMS

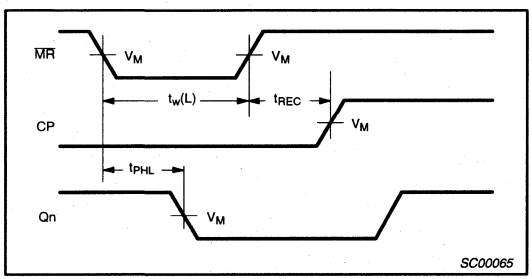
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

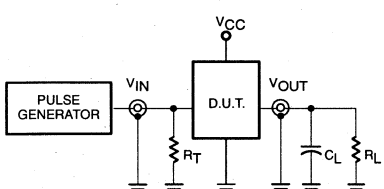


Waveform 3. Data Setup and Hold Times

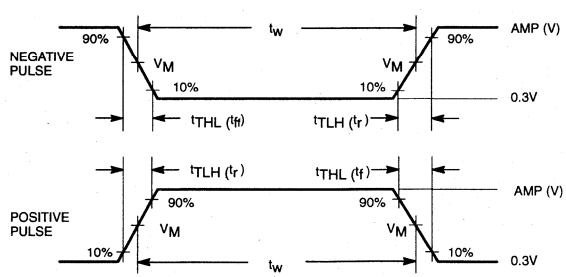


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Latch/flip-flop 74ALS373/74ALS374

74ALS373 Octal transparent latch (3-State)
74ALS374 Octal D flip-flop (3-State)

FEATURES

- 8-bit transparent latch – 74ALS373
- 8-bit positive edge triggered register – 74ALS374
- 3-State output buffers
- Common 3-State output register
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS373	6.0ns	14mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS374	50MHz	17mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin plastic DIP	74ALS373N, 74ALS374N	SOT146-1
20-pin plastic SOL	74ALS373D, 74ALS374D	SOT163-1
20-pin plastic SSOP Type II	74ALS373DB, 74ALS374DB	SOT339-1

DESCRIPTION

The 74ALS373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-Low output enable (OE) controls all eight 3-State buffers independent of the latch operation. When OE is Low, latched or transparent data appears at the output.

When OE is High, the outputs are in High impedance "off" state, which means they will neither drive nor load the bus.

The 74ALS374 is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable (OE) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

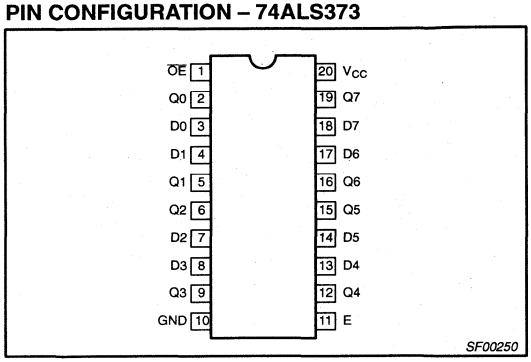
The active-Low output enable (OE) controls all eight 3-State buffers independent of the register operation. When OE is Low, the data in the register appears at the outputs. When OE is High, the outputs are in High impedance "off" state, which means they will neither drive nor load the bus.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

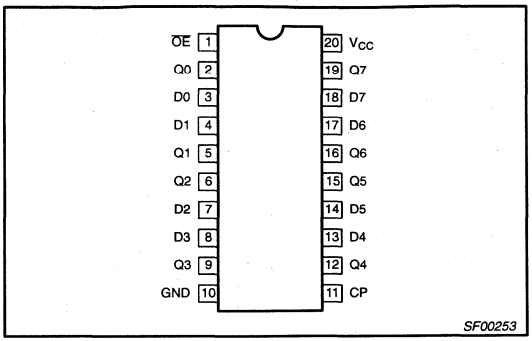
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/1.0	20µA/0.1mA
E (74ALS373)	Enable input (active-High)	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output enable inputs (active-Low)	1.0/1.0	20µA/0.1mA
CP (74ALS374)	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
Q0 – Q7	3-State outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

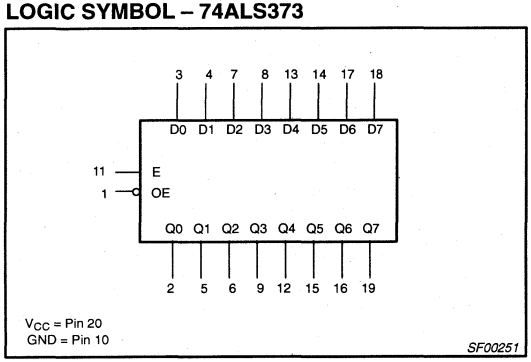
PIN CONFIGURATION – 74ALS373



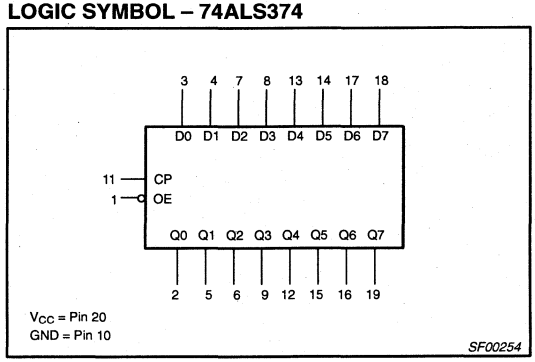
PIN CONFIGURATION – 74ALS374



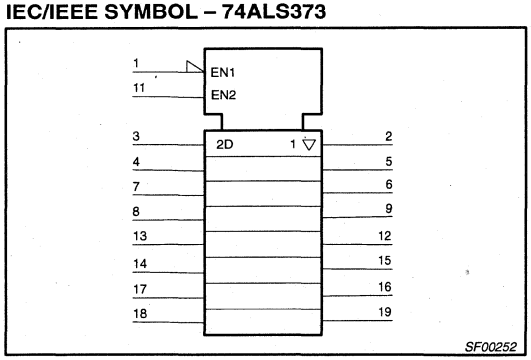
LOGIC SYMBOL – 74ALS373



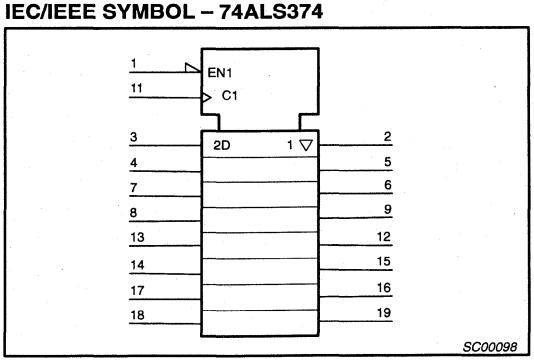
LOGIC SYMBOL – 74ALS374



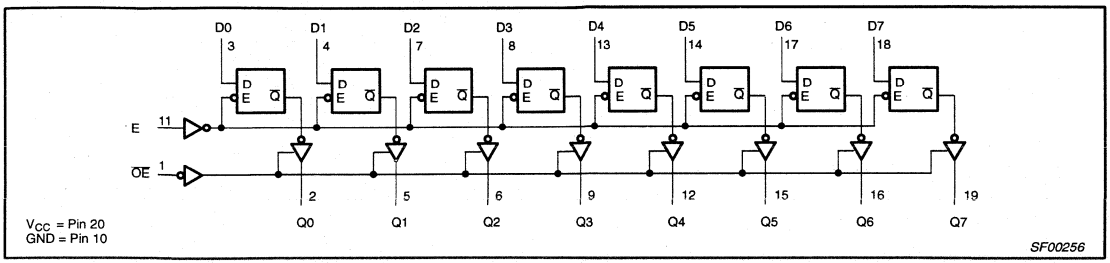
IEC/IEEE SYMBOL – 74ALS373



IEC/IEEE SYMBOL – 74ALS374



LOGIC DIAGRAM – 74ALS373

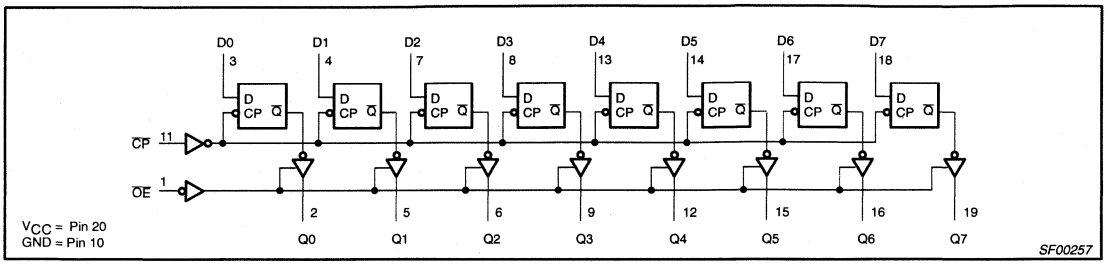


FUNCTION TABLE – 74ALS373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 – Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High-voltage level
h = High state must be present one setup time before the High-to-Low enable transition
L = Low-voltage level
l = Low state must be present one setup time before the High-to-Low enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low enable transition

LOGIC DIAGRAM – 74ALS374



FUNCTION TABLE – 74ALS374

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
					I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	74ALS373		V_{CC} = MAX, V_I = 0.4V				−0.1	mA
		74ALS374						−0.2	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_I = 0.4V				−20	µA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	74ALS373	I_{CCH}	V_{CC} = MAX			7	16	mA
			I_{CCL}				14	25	mA
			I_{CCZ}				17	27	mA
		74ALS374	I_{CCH}	V_{CC} = MAX			11	19	mA
			I_{CCL}				19	29	mA
			I_{CCZ}				20	31	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

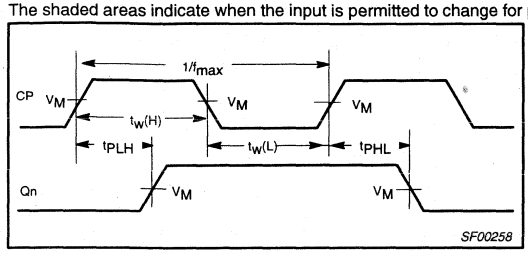
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74ALS373	Waveform 3	2.0 2.0	12.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	3.0 3.0	14.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 3.0	14.0 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	10.0 12.0	ns
f_{MAX}	Maximum clock frequency	74ALS374	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.0 4.0	12.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	3.0 3.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 6 Waveform 7	2.0 3.0	10.0 12.0	ns

AC SETUP REQUIREMENTS

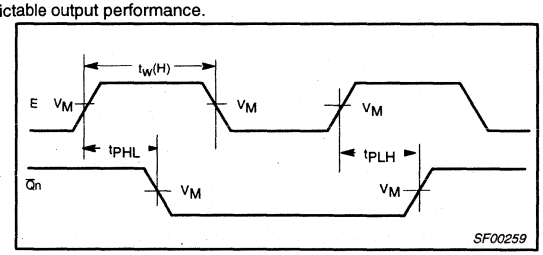
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to E	74ALS373	Waveform 4	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E		Waveform 4	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 2	10.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	74ALS374	Waveform 5	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP		Waveform 5	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	10.0 10.0		ns

AC WAVEFORMS

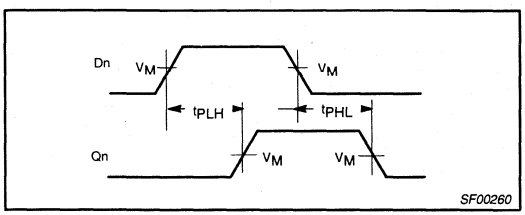
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



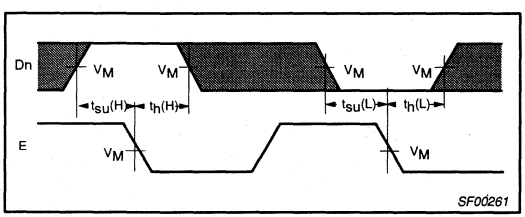
Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency



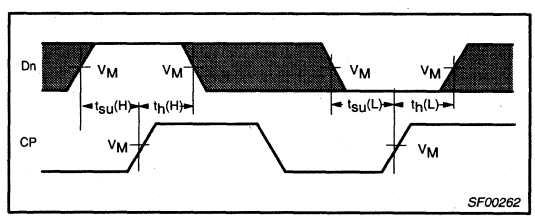
Waveform 2. Propagation Delay for Enable to Output and Enable Pulse Width



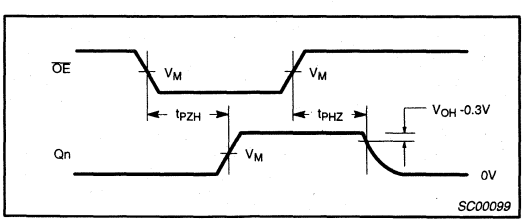
Waveform 3. Propagation Delay for Data to Output



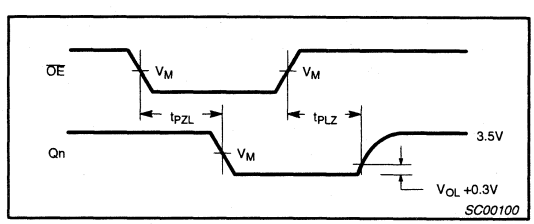
Waveform 4. Data Setup Time and Hold Times



Waveform 5. Data Setup Time and Hold Times

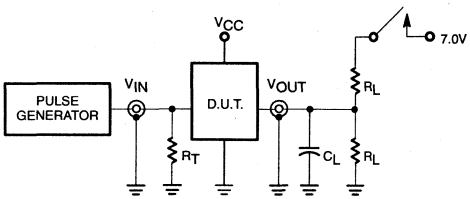


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

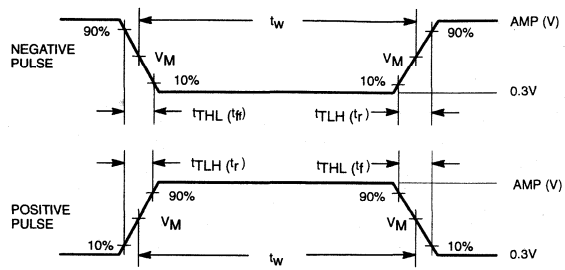
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Octal D flip-flop with enable | 74ALS377

FEATURES

- Ideal for addressable register applications
- Enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- See 74ALS273 for master reset version
- See 74ALS373 for transparent latch version
- See 74ALS374 for 3-State version

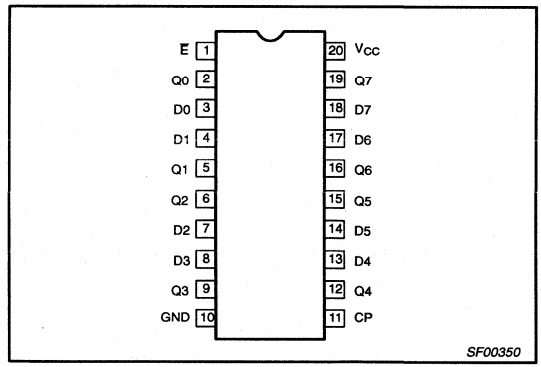
DESCRIPTION

The 74ALS377 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS377	95MHz	15mA

PIN CONFIGURATION



ORDERING INFORMATION

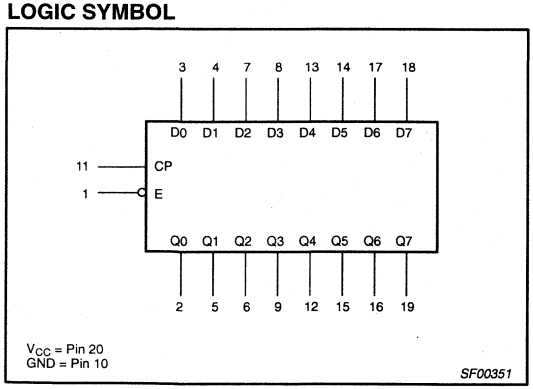
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS377N	SOT146-1
20-pin plastic SOL	74ALS377D	SOT163-1
20-pin plastic SSOP Type II	74ALS377DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

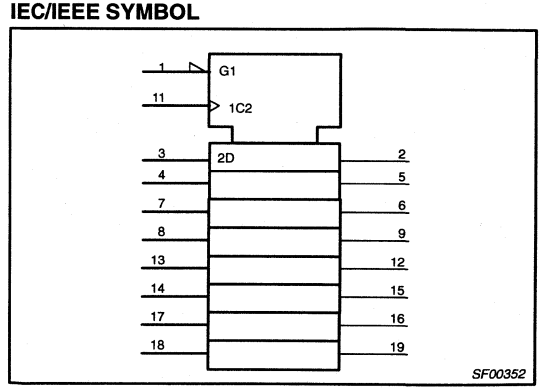
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/2.0	20µA/0.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{E}$	Latch enable input	1.0/1.0	20µA/0.1mA
Q0 – Q7	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

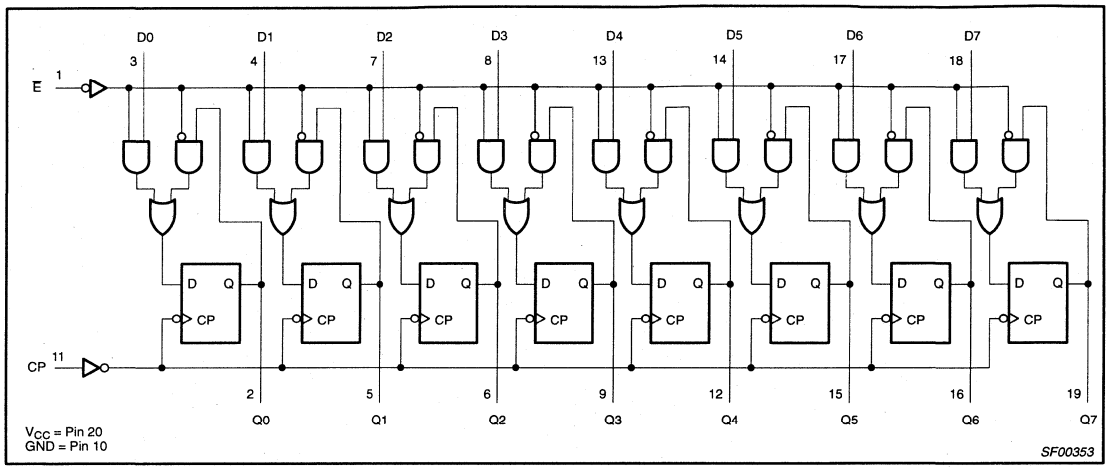
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h	↑	X	NC	Hold (do nothing)
H	X	X	NC	

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
NC= No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
				I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{E}$, CP	V_{CC} = MAX, V_I = 0.4V				−0.1	mA
		Dn					−0.2	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			12	18	mA
		I_{CCL}				20	29	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	65		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.0 3.0	8.0 11.0	ns

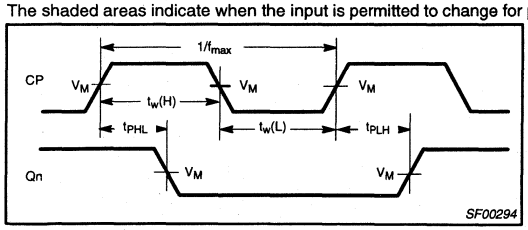
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	Waveform 2	5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 2	0.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	3.0 3.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	6.0 8.0		ns

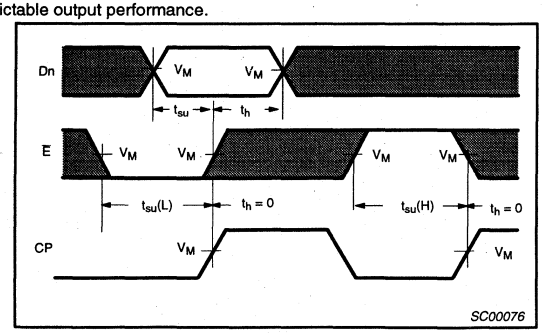
AC WAVEFORMS

For all waveforms, V_M = 1.3V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

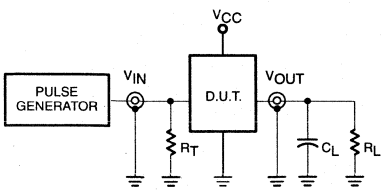


Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

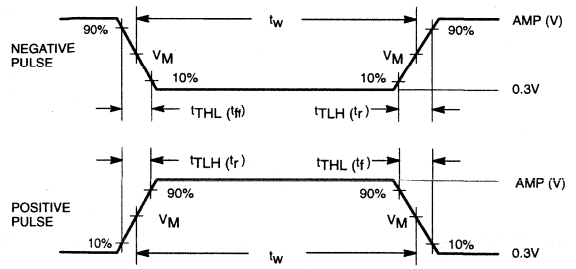


Waveform 2. Data and Enable Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

Latch/flip-flop | 74ALS563A/74ALS564A

74ALS563A Octal transparent latch, inverting (3-State)
74ALS564A Octal D flip-flop, inverting (3-State)

FEATURES

- 74ALS563A is broadside pinout and inverting version of 74ALS373
- 74ALS564A is broadside pinout and inverting version of 74ALS374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- 74ALS573A and 74ALS574A are non-inverting version of 74ALS563B and 74ALS564A respectively

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS563A	6.0ns	12mA
74ALS564A	6.0ns	15mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin plastic DIP	74ALS563AN, 74ALS564AN	SOT146-1
20-pin plastic SOL	74ALS563AD, 74ALS564AD	SOT163-1

DESCRIPTION

The 74ALS563A is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The 74ALS563A is a complementary version of the 74ALS373 and has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the inverted data that is present one setup time before the High-to-Low enable transition.

The 74ALS564A is a complementary version of the 74ALS373 and has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The active-Low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, latched or transparent data appears at the output.

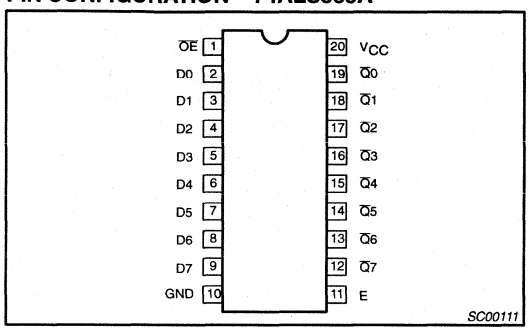
When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

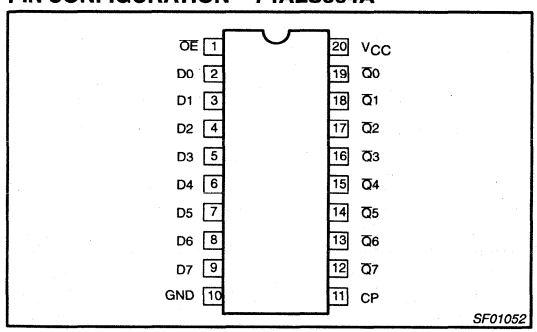
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/2.0	20µA/0.2mA
E (74ALS563A)	Enable input	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20µA/0.1mA
CP (74ALS564A)	Clock pulse input (active rising edge)	1.0/2.0	20µA/0.2mA
$\overline{Q}$0 – $\overline{Q}$7	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

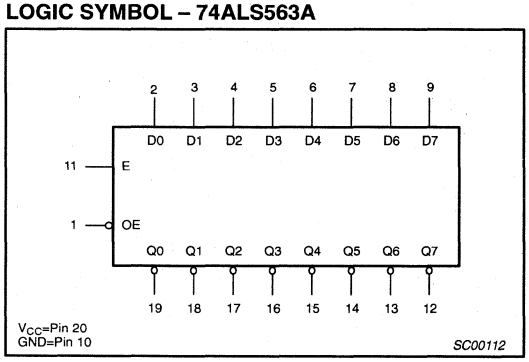
PIN CONFIGURATION – 74ALS563A



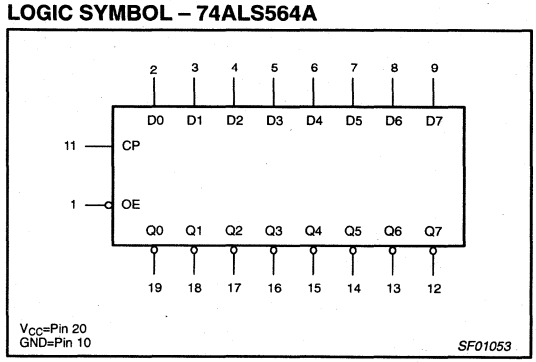
PIN CONFIGURATION – 74ALS564A



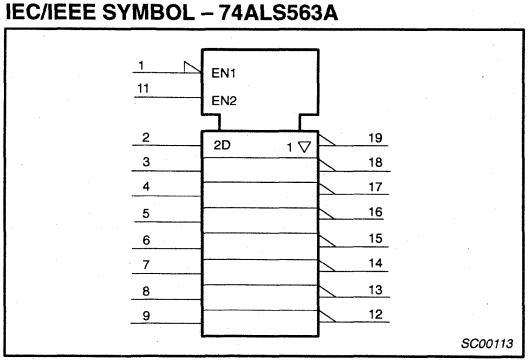
LOGIC SYMBOL – 74ALS563A



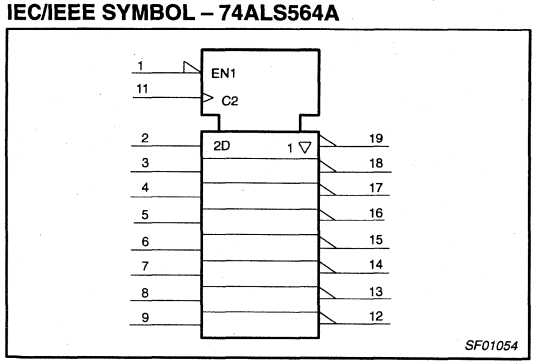
LOGIC SYMBOL – 74ALS564A



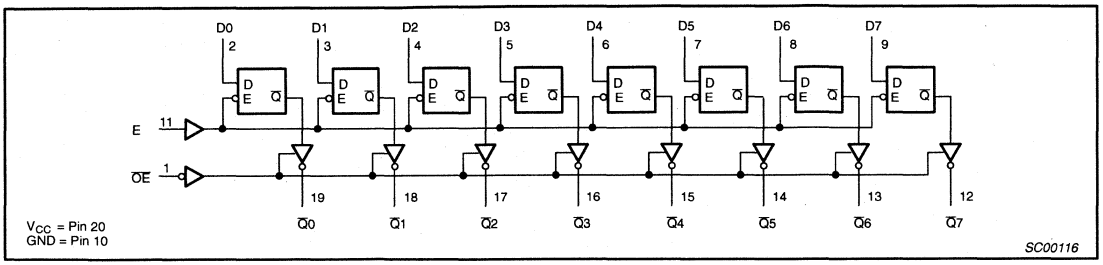
IEC/IEEE SYMBOL – 74ALS563A



IEC/IEEE SYMBOL – 74ALS564A



LOGIC DIAGRAM – 74ALS563A

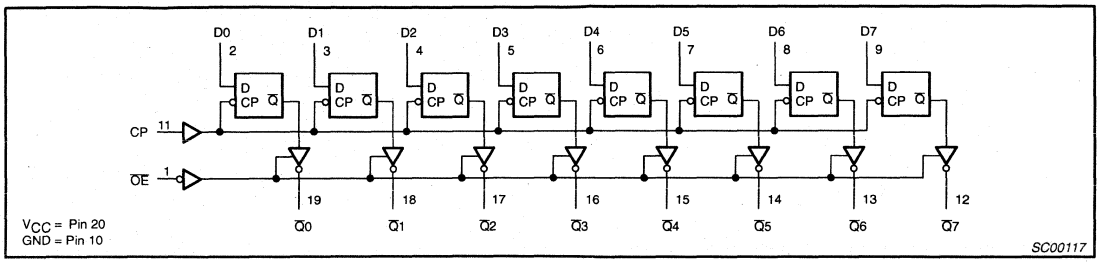


FUNCTION TABLE – 74ALS563A

INPUTS			OUTPUTS REGISTER	INTERNAL	OPERATING MODE
$\overline{OE}$	E	Dn		$\overline{Q0} - \overline{Q7}$	
L	H	L	L	H	Enable and read register
L	H	H	H	L	
L	↓	l	L	H	Latch and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High voltage level
h = High state must be present one setup time before the High-to-Low enable transition
L = Low voltage level
l = Low state must be present one setup time before the High-to-Low enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low enable transition

LOGIC DIAGRAM – 74ALS564A



FUNCTION TABLE – 74ALS564A

INPUTS			OUTPUTS REGISTER	INTERNAL	OPERATING MODE
$\overline{OE}$	CP	Dn		$\overline{Q0} - \overline{Q7}$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
					I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	74ALS563A		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
		74ALS564A						–0.2	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	74ALS563A	I_{CCH}	V_{CC} = MAX			7	12	mA
			I_{CCL}				13	21	mA
			I_{CCZ}				15	24	mA
		74ALS564A	I_{CCH}	V_{CC} = MAX			11	18	mA
			I_{CCL}				17	27	mA
			I_{CCZ}				18	28	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

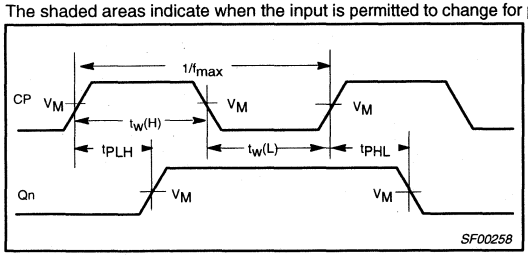
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74ALS563A	Waveform 3	2.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}$n		Waveform 2	4.0 4.0	13.0 13.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	1.0 3.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 6 Waveform 7	1.0 2.0	9.0 11.0	ns
f_{MAX}	Maximum clock frequency	74ALS564A	Waveform 1	45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n		Waveform 1	3.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	1.0 3.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 6 Waveform 7	1.0 2.0	9.0 11.0	ns

AC SETUP REQUIREMENTS

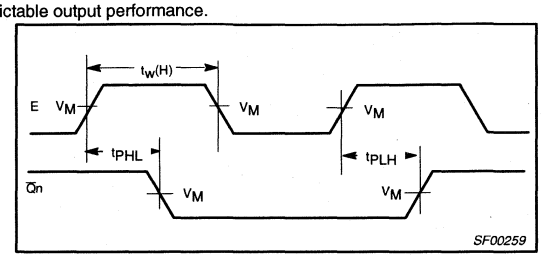
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to E	74ALS563A	Waveform 4	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E		Waveform 4	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	10.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	74ALS564A	Waveform 5	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP		Waveform 5	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 5	7.0 11.0		ns

AC WAVEFORMS

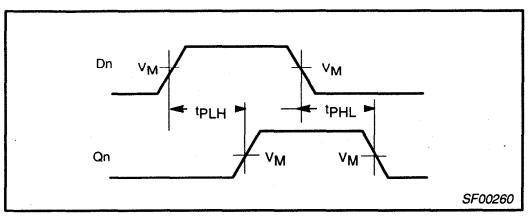
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



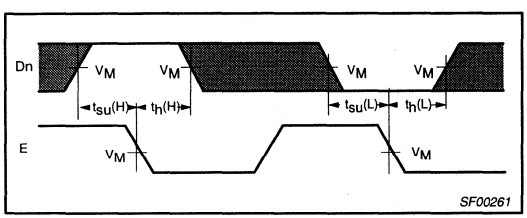
Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency



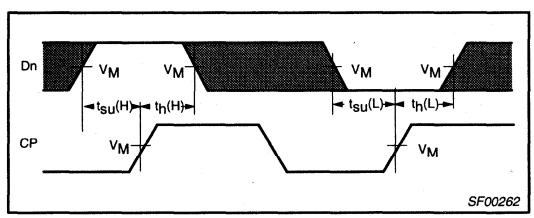
Waveform 2. Propagation Delay for Enable to Output and Enable Pulse Width



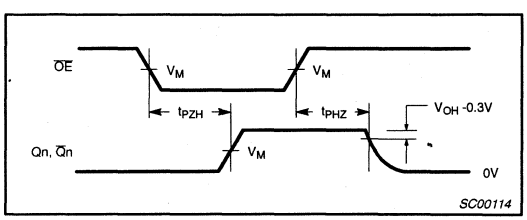
Waveform 3. Propagation Delay for Data to Output



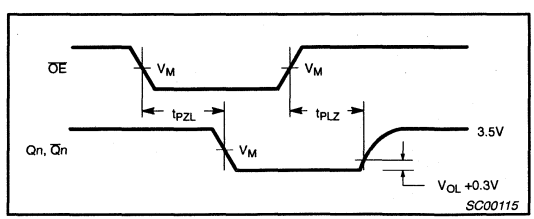
Waveform 4. Data Setup Time and Hold Times



Waveform 5. Data Setup Time and Hold Times

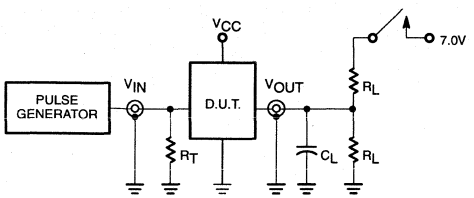


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

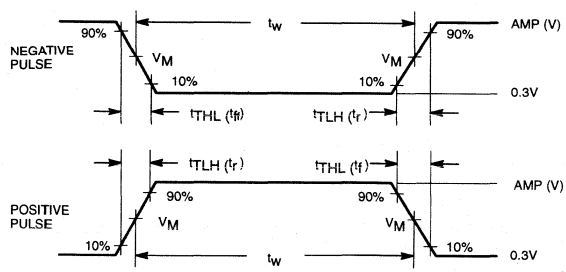
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Latch/flip-flop 74ALS573B/74ALS574A

74ALS573B Octal transparent latch (3-State)
74ALS574A Octal D flip-flop (3-State)

FEATURES

- 74ALS573B is broadside pinout version of 74ALS373
- 74ALS574A is broadside pinout version of 74ALS374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- 74ALS563A and 74ALS564A are inverting version of 74ALS573B and 74ALS574A respectively

DESCRIPTION

The 74ALS573B is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The 74ALS573B is functionally identical to the 74ALS373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 74ALS574A is functionally identical to the 74ALS374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The active-Low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, latched or transparent data appears at the output.

When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS573B	5.0ns	12mA
74ALS574A	6.0ns	15mA

ORDERING INFORMATION

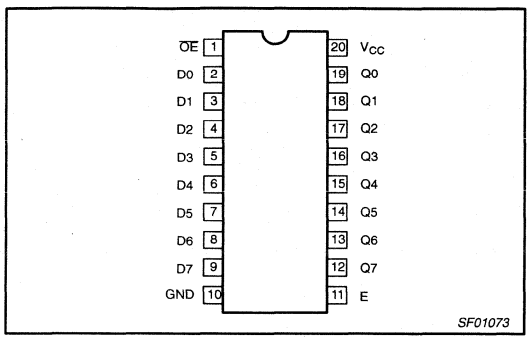
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS573BN, 74ALS574AN	SOT146-1
20-pin plastic SOL	74ALS573BD, 74ALS574AD	SOT163-1
20-pin plastic SSOP Type II	74ALS573BDB, 74ALS574ADB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

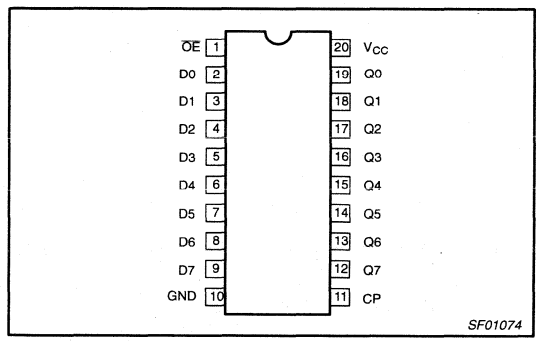
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/1.0	20µA/0.2mA
E (74ALS573B)	Latch enable input	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20µA/0.1mA
CP (74ALS574A)	Clock pulse input (active rising edge)	1.0/2.0	20µA/0.2mA
Q0 – Q7	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

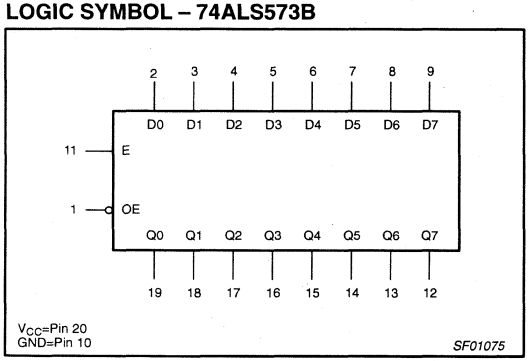
PIN CONFIGURATION – 74ALS573B



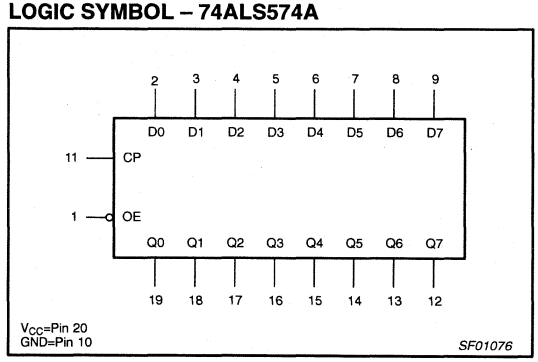
PIN CONFIGURATION – 74ALS574A



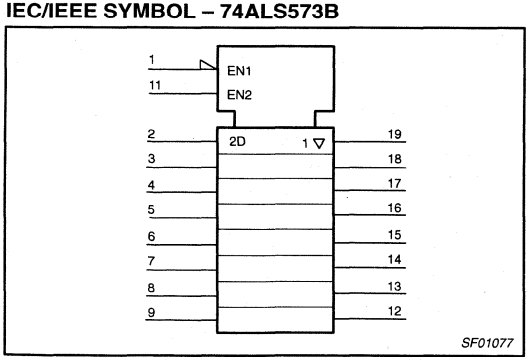
LOGIC SYMBOL – 74ALS573B



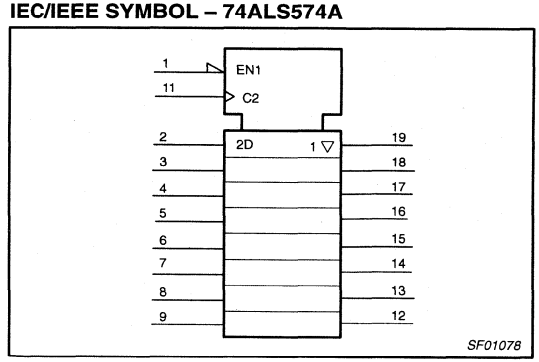
LOGIC SYMBOL – 74ALS574A



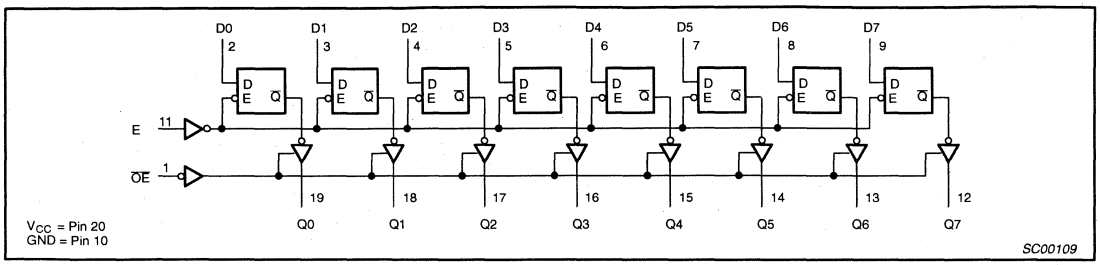
IEC/IEEE SYMBOL – 74ALS573B



IEC/IEEE SYMBOL – 74ALS574A



LOGIC DIAGRAM – 74ALS573B

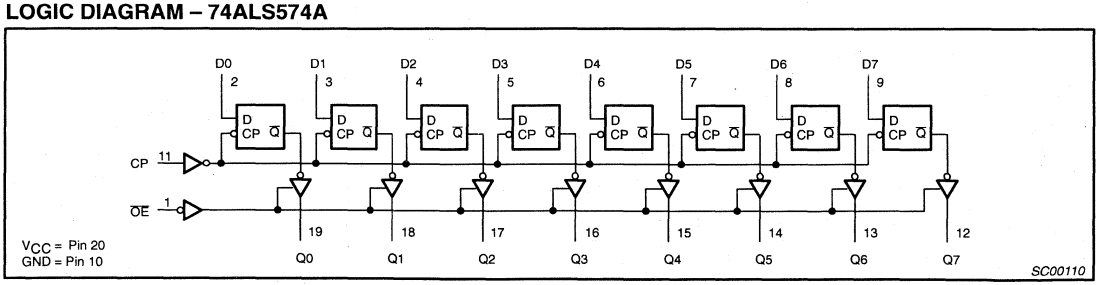


FUNCTION TABLE – 74ALS573B

INPUTS			OUTPUTS REGISTER	INTERNAL	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 – Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High-voltage level
h = High state must be present one setup time before the High-to-Low enable transition
L = Low-voltage level
l = Low state must be present one setup time before the High-to-Low enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low enable transition

LOGIC DIAGRAM – 74ALS574A



FUNCTION TABLE – 74ALS574A

INPUTS			OUTPUTS REGISTER	INTERNAL	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Latch and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
					I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at minimum input voltage			V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	74ALS573B		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
		74ALS574A		V_{CC} = MAX, V_I = 0.4V				–0.2	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_I = 0.4V				–20	µA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	74ALS573B	I_{CCH}	V_{CC} = MAX			7	12	mA
			I_{CCL}				13	21	mA
			I_{CCZ}				15	24	mA
		74ALS574A	I_{CCH}	V_{CC} = MAX			10	16	mA
			I_{CCL}				17	27	mA
			I_{CCZ}				18	28	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

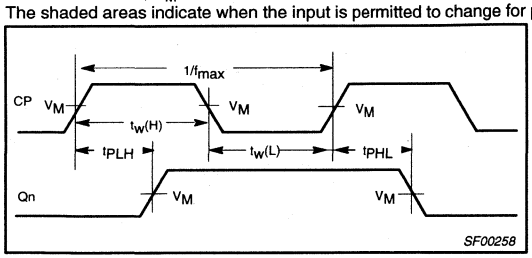
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74ALS573B	Waveform 3	2.0 2.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	4.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 6 Waveform 7	1.0 2.0	9.0 11.0	ns
f_{MAX}	Maximum clock frequency	74ALS574A	Waveform 1	45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 6 Waveform 7	1.0 2.0	9.0 11.0	ns

AC SETUP CHARACTERISTICS

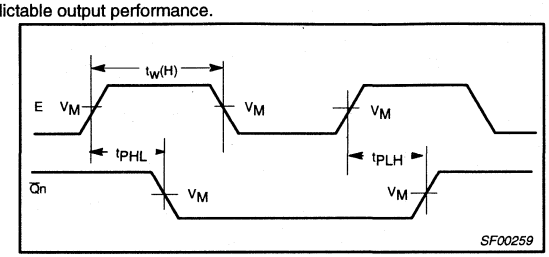
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to E	74ALS573B	Waveform 4	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E		Waveform 4	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	10.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	74ALS574A	Waveform 5	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP		Waveform 5	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 5	8.0 12.0		ns

AC WAVEFORMS

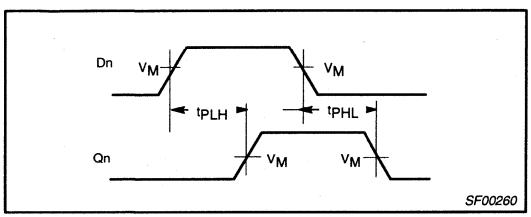
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



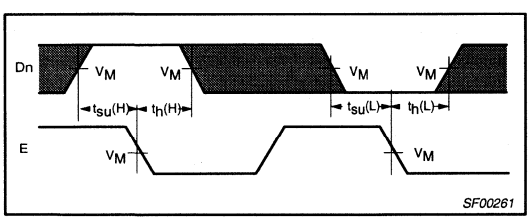
Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency



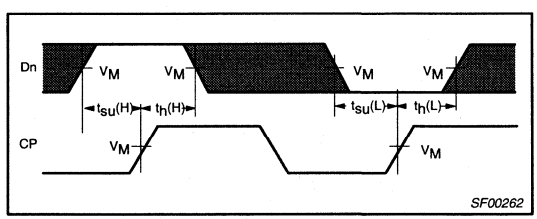
Waveform 2. Propagation Delay for Enable to Output and Enable Pulse Width



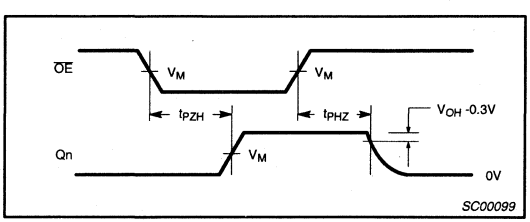
Waveform 3. Propagation Delay for Data to Output



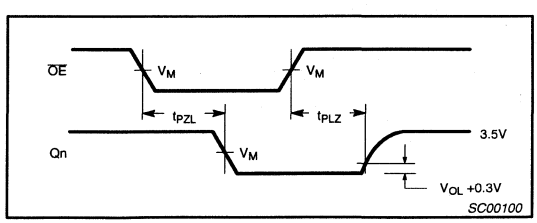
Waveform 4. Data Setup Time and Hold Times



Waveform 5. Data Setup Time and Hold Times

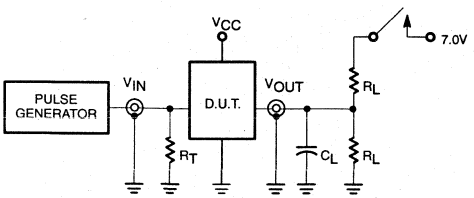


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

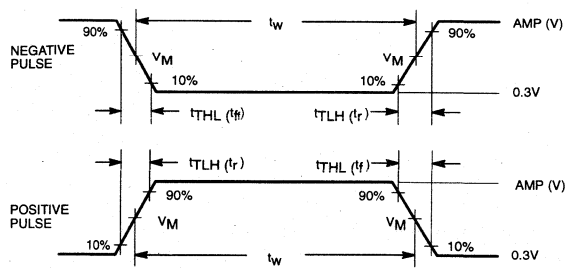
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

74ALS620A/74ALS620A-1 Octal bus transceiver, inverting (3-State)
74ALS623A/74ALS623A-1 Octal bus transceiver, non-inverting (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48mA I_{OL} within the +5% V_{CC} range

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS620A/620A-1	4.0ns	33mA
74ALS623A/623A-1	4.0ns	38mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS620AN, 74ALS620A-1N 74ALS623AN, 74ALS623A-1N	SOT146-1
20-pin plastic SOL	74ALS620AD, 74ALS620A-1D 74ALS623AD, 74ALS623A-1D	SOT163-1

DESCRIPTION

The 74ALS620A and 74ALS623A are octal transceiver featuring 3-State bus compatible outputs in both transmit and receive directions. The 74ALS620A is an inverting version of the 74ALS623A. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

The outputs for the 74ALS620A-1 and 74ALS623A are capable of sinking up to 48mA when within the ±5% V_{CC} range.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

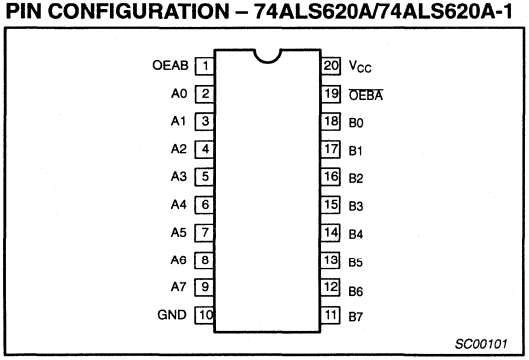
These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending on the logic levels at the enable inputs ($\overline{OEBA}$ and OEAB). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the 74ALS620A and 74ALS623A the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of the bus lines (16 in all) will remain at their last states.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

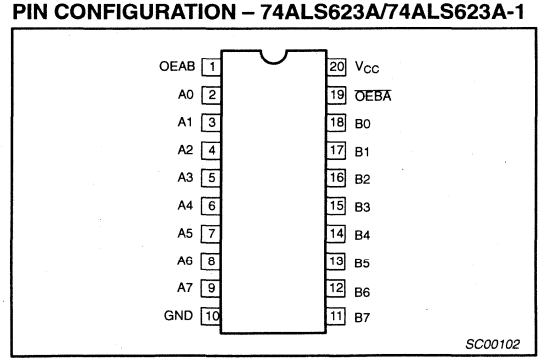
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/1.0	20µA/0.1mA
A0 – A7, B0 – B7	Data outputs	750/240	15mA/24mA
A0 – A7, B0 – B7	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

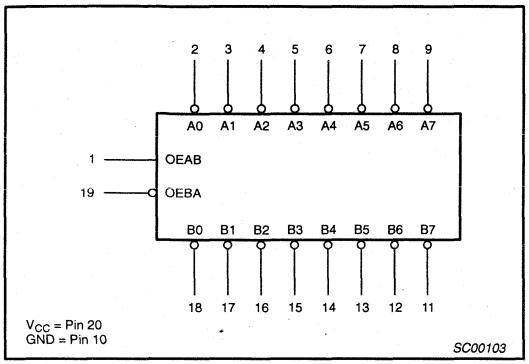
PIN CONFIGURATION – 74ALS620A/74ALS620A-1



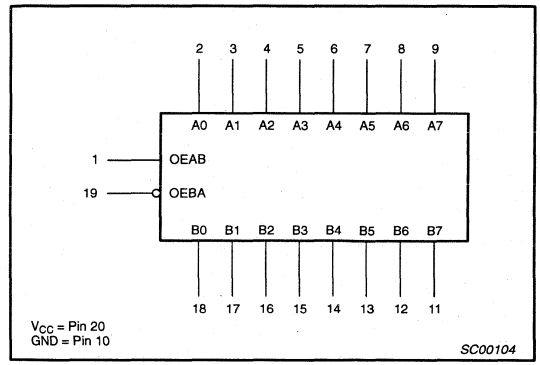
PIN CONFIGURATION – 74ALS623A/74ALS623A-1



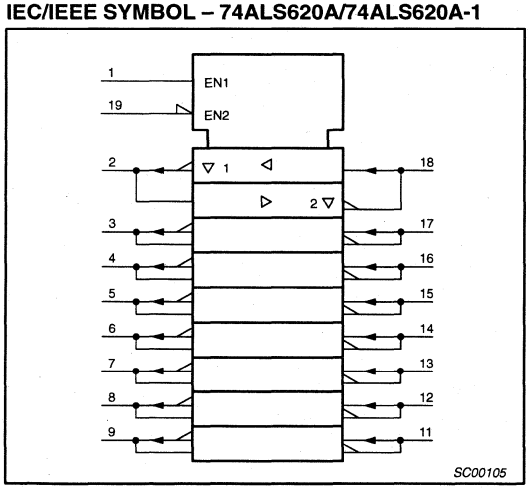
LOGIC SYMBOL – 74ALS620A/74ALS620A-1



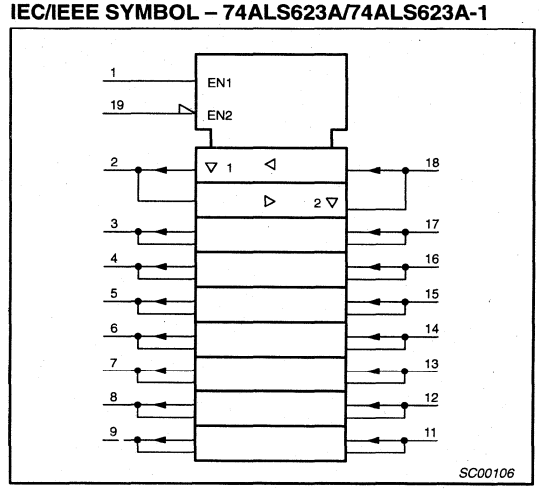
LOGIC SYMBOL – 74ALS623A/74ALS623A-1



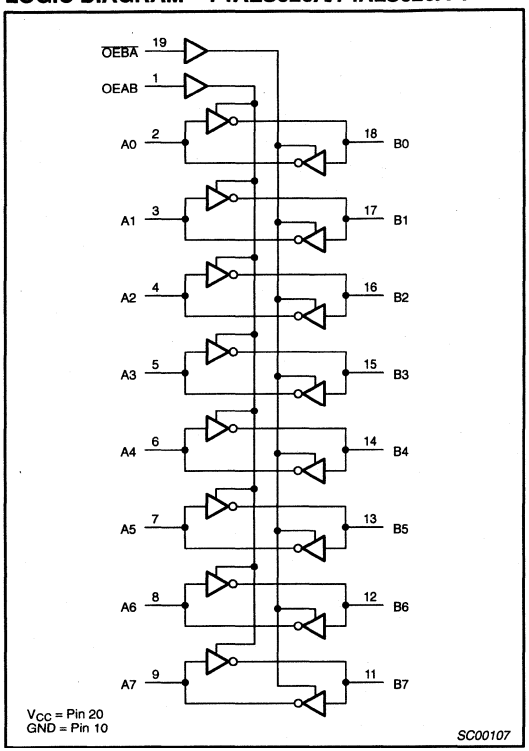
IEC/IEEE SYMBOL – 74ALS620A/74ALS620A-1



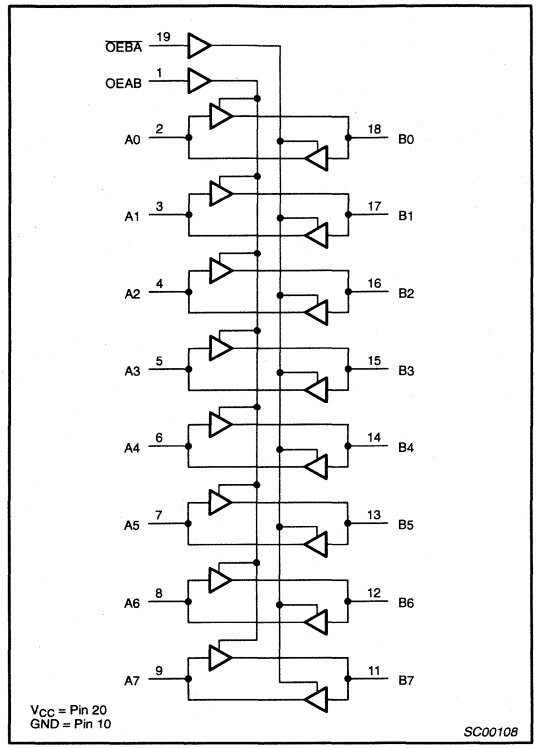
IEC/IEEE SYMBOL – 74ALS623A/74ALS623A-1



LOGIC DIAGRAM – 74ALS620A/74ALS620A-1



LOGIC DIAGRAM – 74ALS623A/74ALS623A-1



FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	74ALS620A	74ALS623A
L	L	$\overline{B}$ data to A Bus	B data to A Bus
L	H	$\overline{A}$ data to B Bus	A data to B Bus
H	L	Z	Z
L	H	$\overline{B}$ data to A Bus	B data to A Bus
L	H	$\overline{A}$ data to B Bus	A data to B Bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48 [1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
					I_{OH} = –3mA	2.4	3.2		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
		–1 versions		V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$ or OEAB		V_{CC} = MAX, V_I = 7.0V				0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_O	Output current[4]			V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	74ALS620A 74ALS620A-1	I_{CCH}	V_{CC} = MAX			24	34	mA
			I_{CCL}				42	49	mA
			I_{CCZ}				45	52	mA
		74ALS623A 74ALS623A-1	I_{CCH}	V_{CC} = MAX			24	43	mA
			I_{CCL}				41	50	mA
			I_{CCZ}				46	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS FOR 74ALS620A/74ALS620A-1

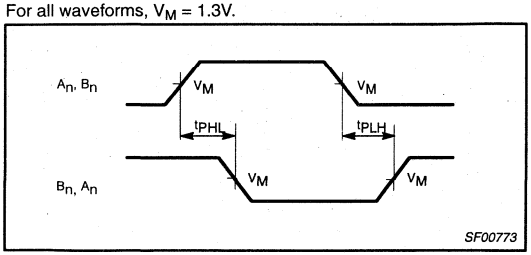
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 3.0	17.0 25.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 2.0	12.0 18.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	18.0 25.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	12.0 18.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74ALS623A/74ALS623A-1

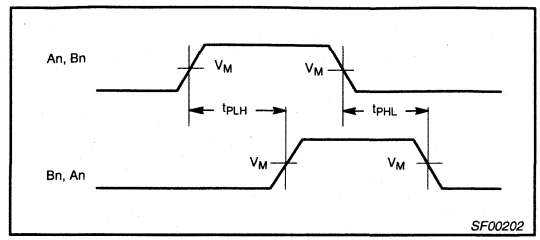
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 2	2.0 2.0	13.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns

AC WAVEFORMS

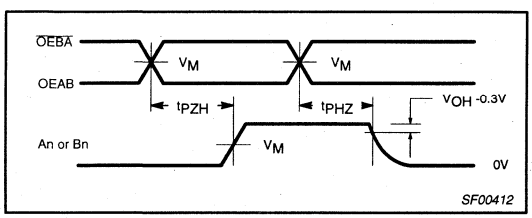
For all waveforms, V_M = 1.3V.



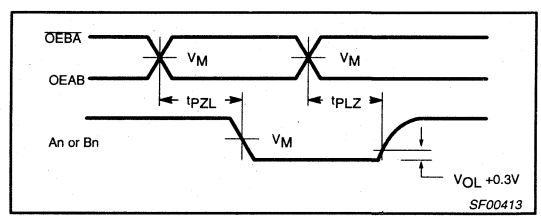
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-inverting Outputs

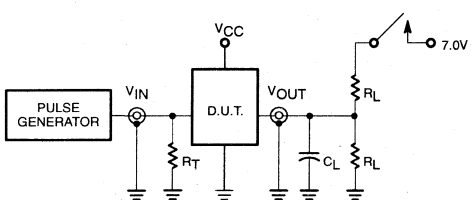


Waveform 3. 3-State Output Enable Time to High Level and Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

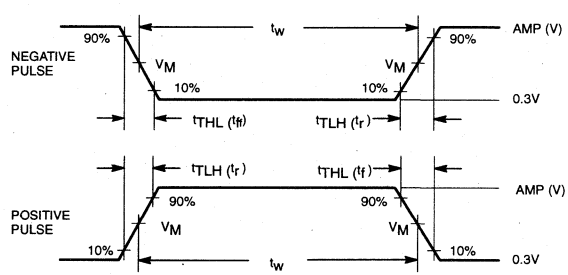
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

Octal transceiver (3-State) 74ALS645A/74ALS645A-1

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- Outputs are placed in high impedance state during power-off conditions
- The -1 version sinks 48mA I_{OL} within the +5% V_{CC} range

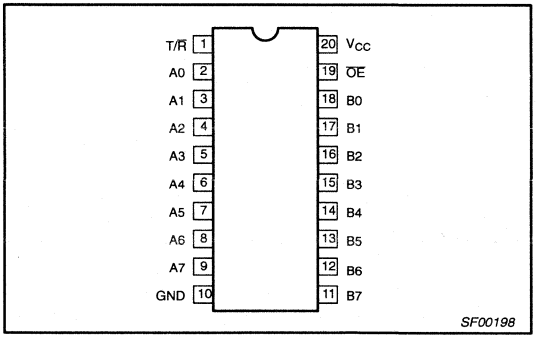
DESCRIPTION

The 74ALS645A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The device features an output enable ($\overline{OE}$) input for easy cascading and transmit/receive (R/$\overline{T}$) input for direction control.

The 74ALS645A-1 is the same as the 74ALS645A except that both ports sink 48mA within the ±5% V_{CC} range.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS645A	7.0ns	34mA
74ALS645A-1	7.0ns	34mA

PIN CONFIGURATION



ORDERING INFORMATION

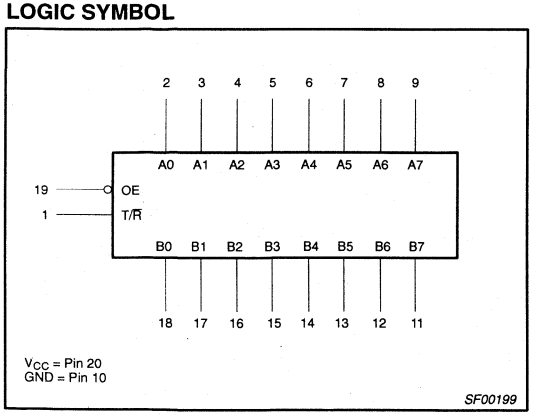
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS645AN, 74ALS645A-1N	SOT146-1
20-pin plastic SOL	74ALS645AD, 744ALS645A-1D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

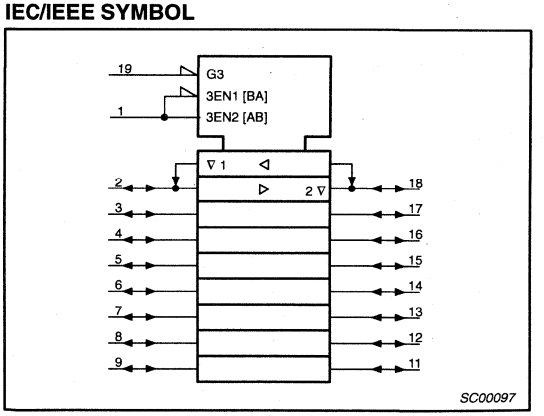
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20µA/0.1mA
T/$\overline{R}$	Transmit/receive input	1.0/1.0	20µA/0.1mA
A0 – A7	A port outputs	750/240	15mA/24mA
B0 – B7	B port outputs	750/240	15mA/24mA
A0 – A7	A port outputs (-1 version)	750/480	15mA/48mA
B0 – B7	B port outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

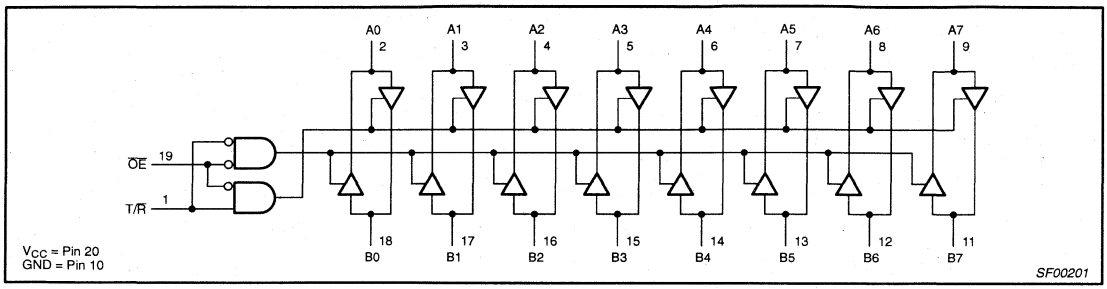
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48[1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTES:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –3mA	2.4	3.2		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
		-1 version	V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	$\overline{OE}$ or T/$\overline{R}$	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		A or B ports	V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current[3]		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current[3]		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_O	Output current[4]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			28	45	mA
		I_{CCL}				40	55	mA
		I_{CCZ}				44	58	mA

NOTES:

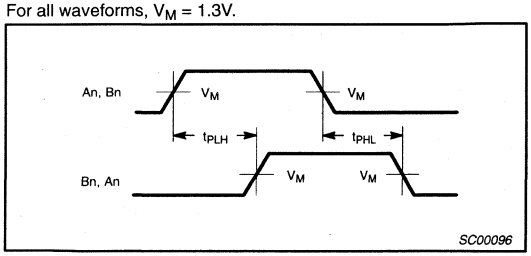
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

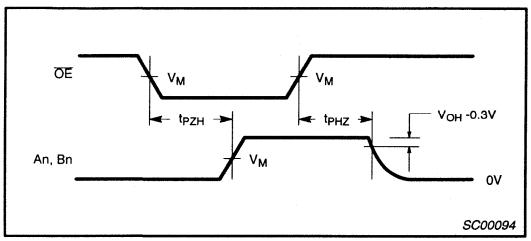
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	20.0 20.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 4.0	10.0 15.0	ns

AC WAVEFORMS

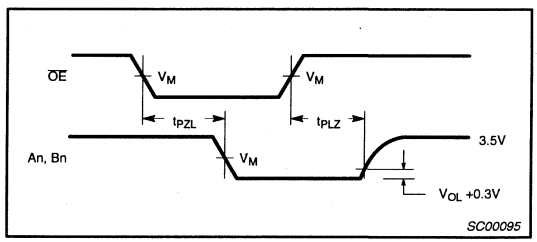
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Non-inverting Outputs

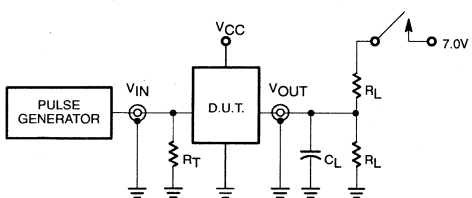


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

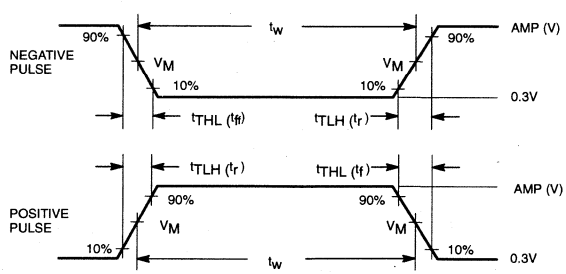
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

Transceiver/register

74ALS646/74ALS646-1
74ALS648/74ALS648-1

74ALS646/646-1 Octal transceiver/register, non-inverting (3-State)
74ALS648/648-1 Octal transceiver/register, inverting (3-State)

FEATURES

- Combines 74ALS245 and two 74ALS374 type functions in one chip
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- 3-State outputs
- The -1 version sink 48mA I_{OL} within the ±5% V_{CC} range

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS646/646-1	140MHz	48mA
74ALS648/648-1	140MHz	54mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
24-pin plastic DIP	74ALS646N, 74ALS646-1N, 74ALS648N, 74ALS648-1N	SOT222-1
24-pin plastic SOL	74ALS646D, 74ALS646-1D, 74ALS648D, 74ALS648-1D	SOT137-1

DESCRIPTION

The 74ALS646/74ALS646-1 and 74ALS648/74ALS648-1 transceivers/registers consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output enable ($\overline{OE}$) and direction (DIR) and select (SAB, SBA) pins are provided for bus management.

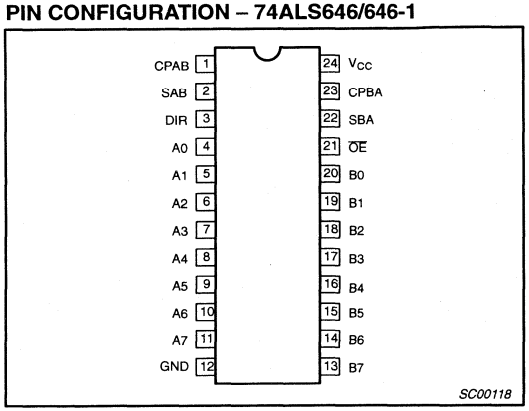
The 74ALS646-1 and 74ALS648-1 will sink 48mA if the V_{CC} is limited to 5.0V ±0.25V.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

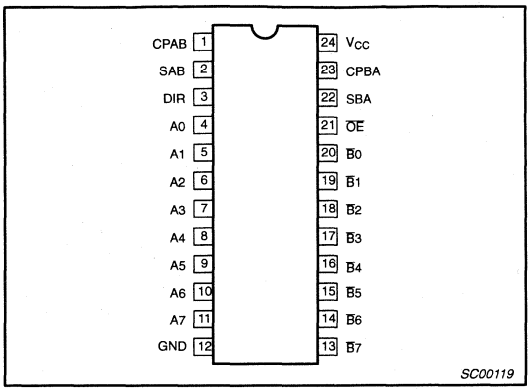
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	A inputs	1.0/1.0	20µA/0.1mA
B0 – B7	B inputs	1.0/1.0	20µA/0.1mA
$\overline{CPAB}$	A-to-B clock input	1.0/1.0	20µA/0.1mA
CPBA	B-to-A clock input	1.0/1.0	20µA/0.1mA
SAB	A-to-B select input	1.0/1.0	20µA/0.1mA
SBA	B-to-A select input	1.0/1.0	20µA/0.1mA
DIR	Data flow directional control input	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output enable input	1.0/1.0	20µA/0.1mA
A0 – A7, B0 – B7	Data outputs	750/240	15mA/24mA
A0 – A7, B0 – B7	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

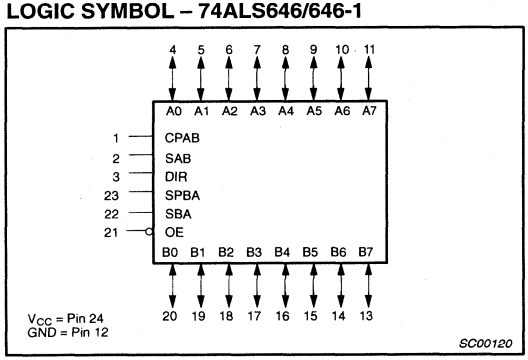
PIN CONFIGURATION – 74ALS646/646-1



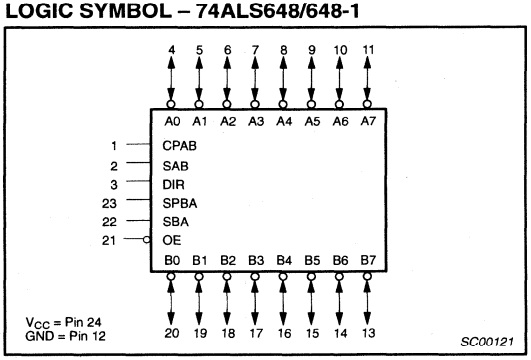
PIN CONFIGURATION – 74ALS648/648-1



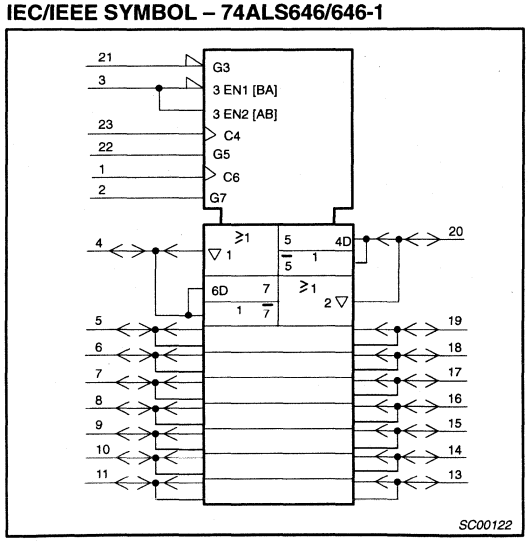
LOGIC SYMBOL – 74ALS646/646-1



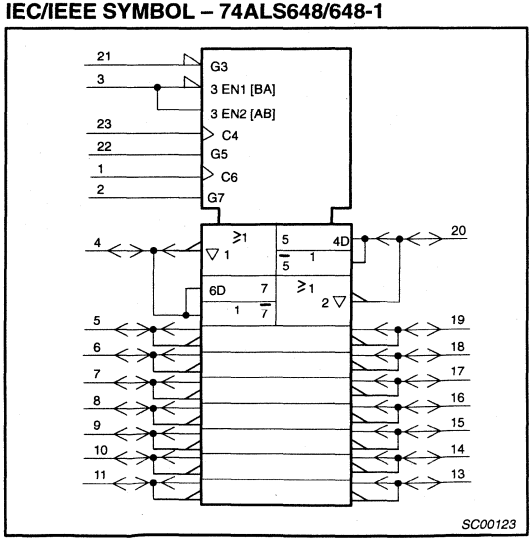
LOGIC SYMBOL – 74ALS648/648-1



IEC/IEEE SYMBOL – 74ALS646/646-1



IEC/IEEE SYMBOL – 74ALS648/648-1

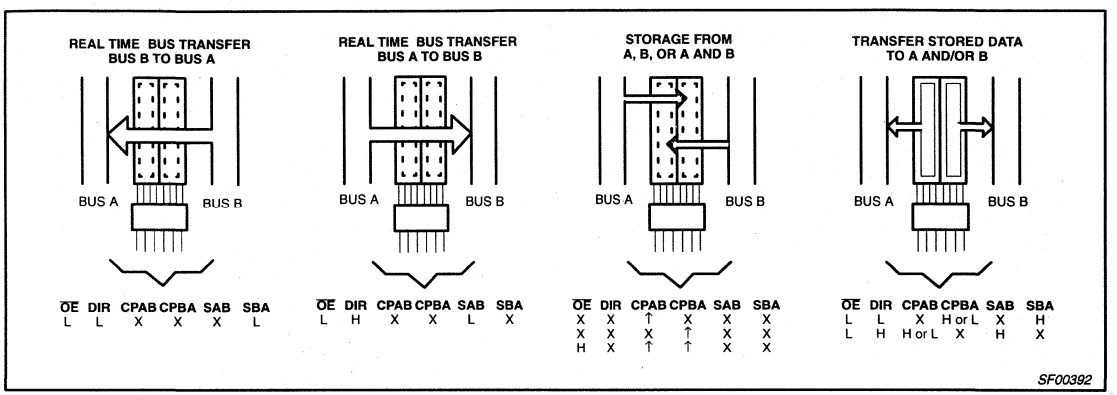


BUS MANAGEMENT FUNCTIONS

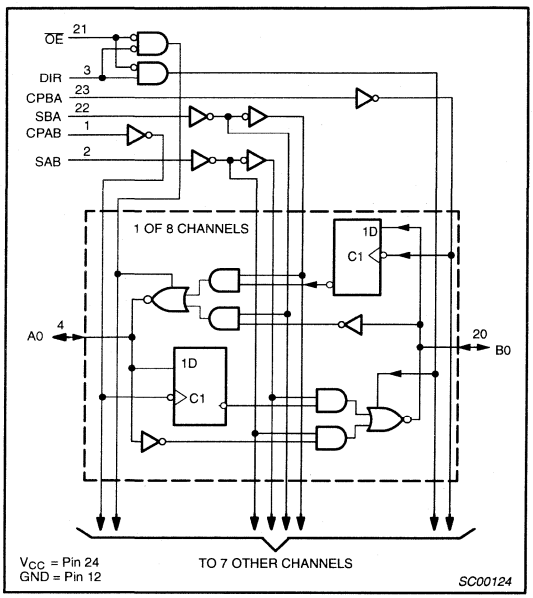
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALS646/646-1 and 74ALS648/648-1.

The select pins determine whether data is stored or transferred through the device in real time.

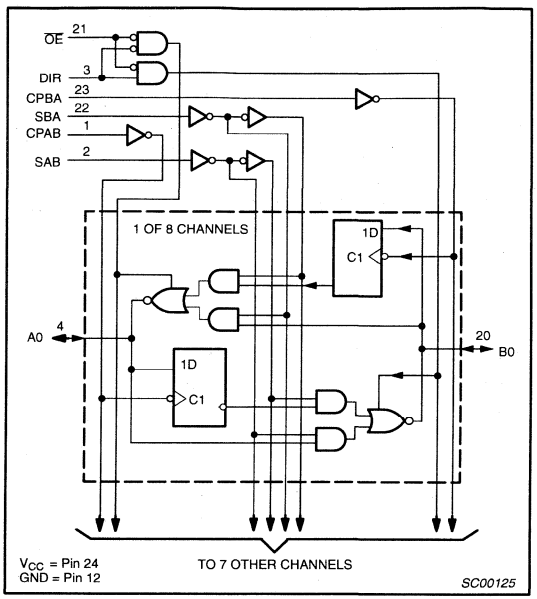
The DIR determines which bus will receive data when the OE pin is Low.



LOGIC SYMBOL – 74ALS646/646-1



LOGIC SYMBOL – 74ALS648/648-1



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	74ALS646/74ALS646-1	74ALS648/74ALS648-1
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus	Stored $\overline{A}$ data to B bus

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48 [1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = –3mA	2.4	3.2		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
		-1 versions	V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	control inputs	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		A or B ports	V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current[3]		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current[3]		V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_O	Output current[4]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	57	mA
		I_{CCL}				53	78	mA
		I_{CCZ}				51	72	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS FOR 74ALS646/74ALS646-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		UNIT
			MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	Waveform 1	5.0 6.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2, 3	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B Low)	Waveform 2, 3	5.0 5.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B High)	Waveform 2, 3	5.0 5.0	11.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.0 5.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	2.0 3.0	8.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 5.0	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 3.0	10.0 13.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74ALS648/74ALS648-1

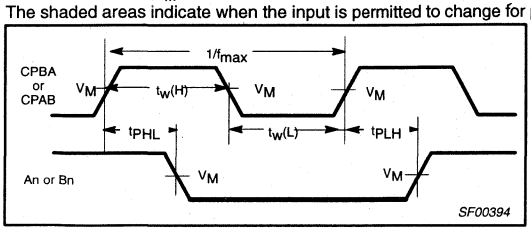
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	Waveform 1	5.0 6.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2, 3	1.0 3.0	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B Low)	Waveform 2, 3	5.0 5.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B High)	Waveform 2, 3	4.0 5.0	11.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	2.0 4.0	8.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	1.0 2.0	8.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.0 5.0	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 2.0	11.0 11.0	ns

AC SETUP REQUIREMENTS

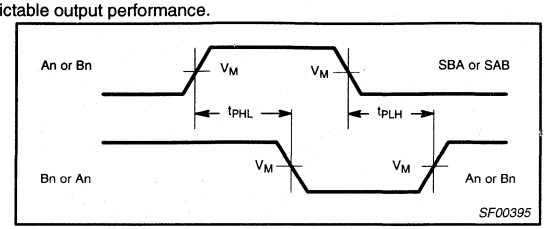
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
t_{su} (H) t_{su} (L)	Setup time, High or Low An or Bn to CPAB or CPBA	Waveform 4	5.0 5.0		ns
t_h (H) t_h (L)	Hold time, High or Low An or Bn to CPAB or CPBA	Waveform 4	0.0 1.0		ns
t_w (H) t_w (L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	6.0 4.0		ns

AC WAVEFORMS

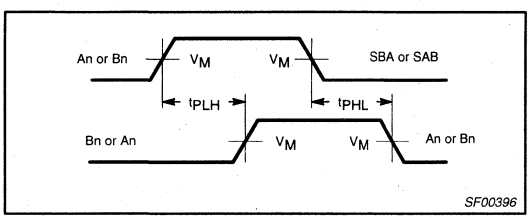
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



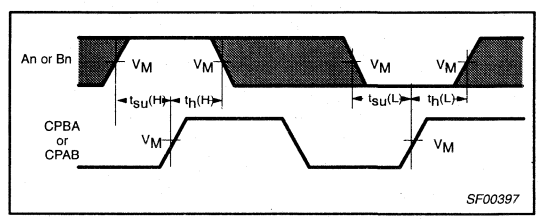
Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



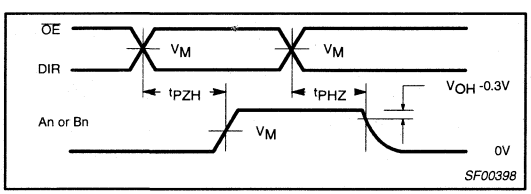
Waveform 2. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn



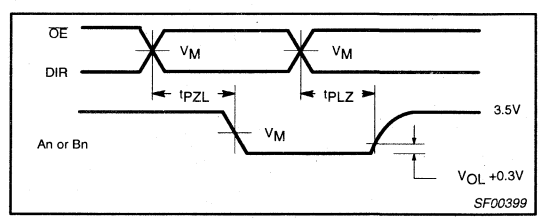
Waveform 3. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn



Waveform 4. Data Setup Time and Hold Times

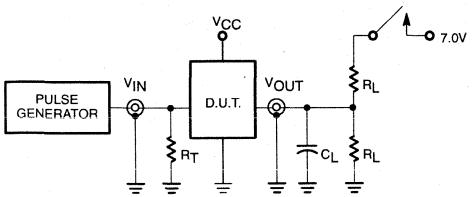


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State and Open Collector Outputs

SWITCH POSITION

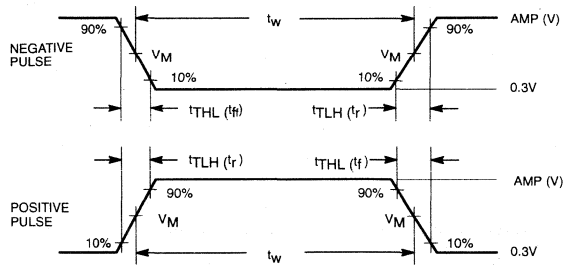
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
open collector	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00126

Transceiver/register

74ALS651/74ALS651-1
74ALS652/74ALS652-1

74ALS651/651-1 Octal transceiver/register, inverting (3-State)
74ALS652/652-1 Octal transceiver/register, non-inverting (3-State)

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- 3-State outputs
- The -1 versions sinks 48mA I_{OL} within the ±5% V_{CC} range

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS651/74ALS651-1	140MHz	40mA
74ALS652/74ALS652-1	140MHz	46mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
24-pin plastic DIP	74ALS651N, 74ALS651-1N, 74ALS652N, 74ALS652-1N	SOT222-1
24-pin plastic SOL	74ALS651D, 74ALS651-1D, 74ALS652D, 74ALS652-1D	SOT137-1

DESCRIPTION

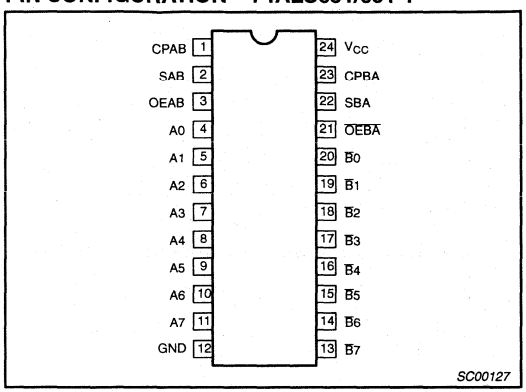
The 74LAS651 and 74ALS652 transceivers/registers consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output enable (OEAB, $\overline{OEBA}$) and select (SAB, SBA) pins are provided for bus management. The 74LAS651-1 and 74ALS652-1 will sink 48mA if the V_{CC} is limited to 5.0V ± 0.25V.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

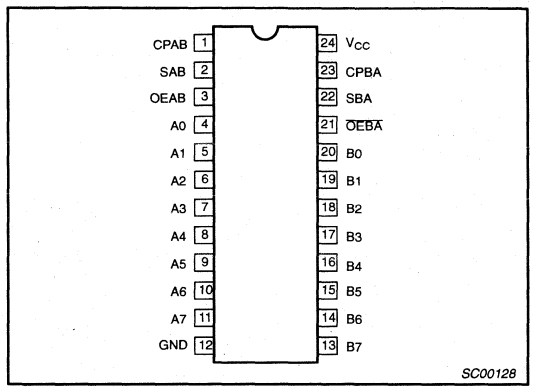
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	A inputs	1.0/1.0	70µA/0.1mA
B0 – B7	B inputs	1.0/1.0	70µA/0.1mA
CPAB	A-to-B clock input	1.0/1.0	20µA/0.1mA
CPBA	B-to-A clock input	1.0/1.0	20µA/0.1mA
SAB	A-to-B select input	1.0/1.0	20µA/0.1mA
SBA	B-to-A select input	1.0/1.0	20µA/0.1mA
OEAB	A-to-B output enable input	1.0/1.0	20µA/0.1mA
$\overline{OEBA}$	B-to-A output enable input	1.0/1.0	20µA/0.1mA
A0 – A7, B0 – B7	A, B outputs	750/240	15mA/24mA
A0 – A7, B0 – B7	A, B outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

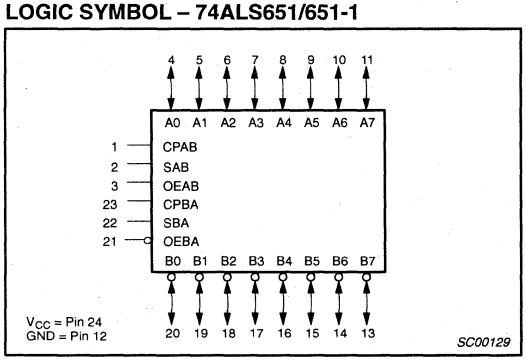
PIN CONFIGURATION – 74ALS651/651-1



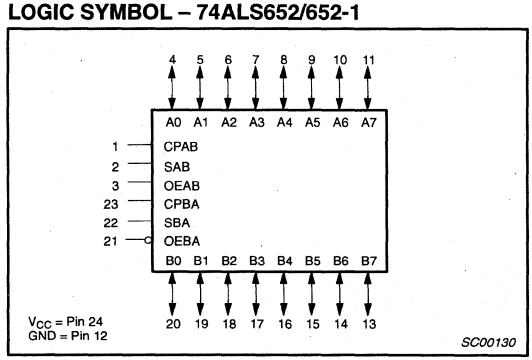
PIN CONFIGURATION – 74ALS652/652-1



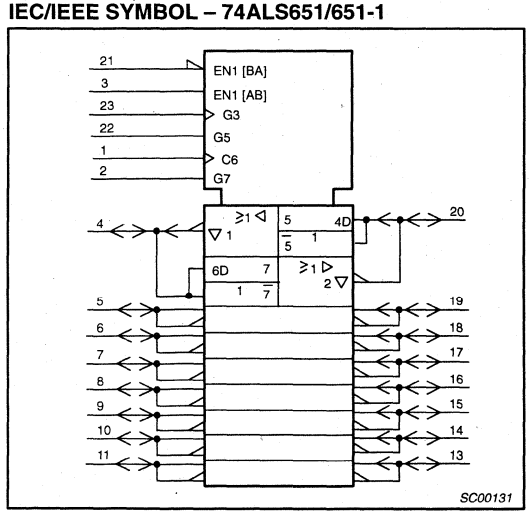
LOGIC SYMBOL – 74ALS651/651-1



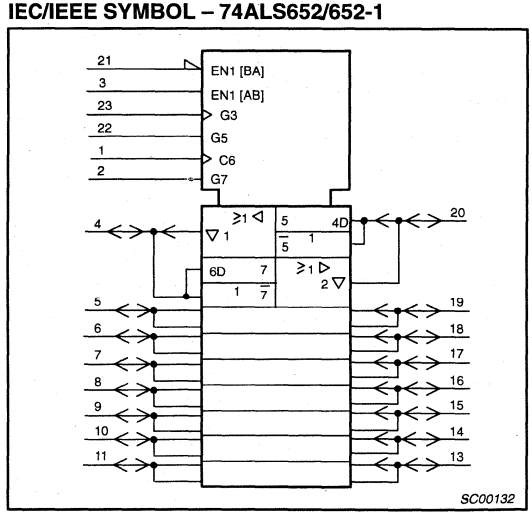
LOGIC SYMBOL – 74ALS652/652-1



IEC/IEEE SYMBOL – 74ALS651/651-1

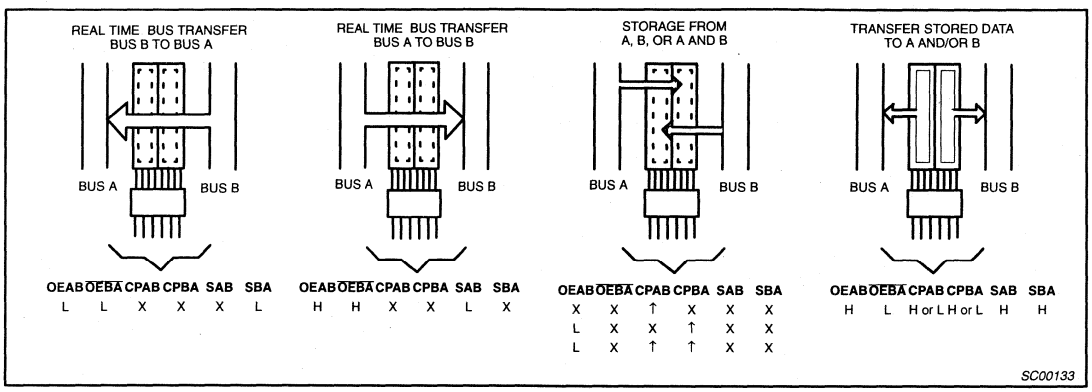


IEC/IEEE SYMBOL – 74ALS652/652-1

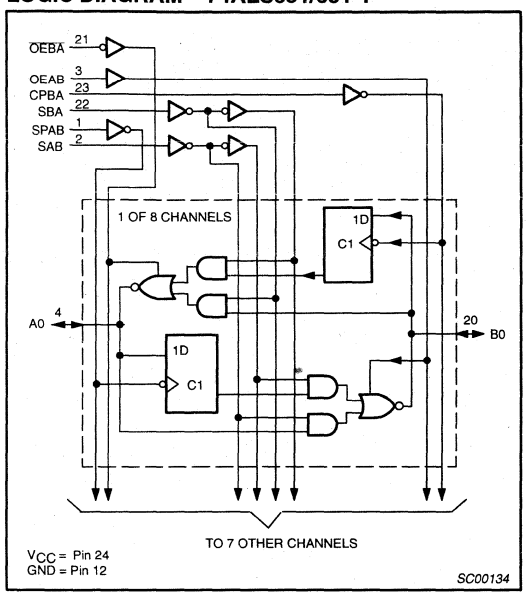


BUS MANAGEMENT FUNCTIONS

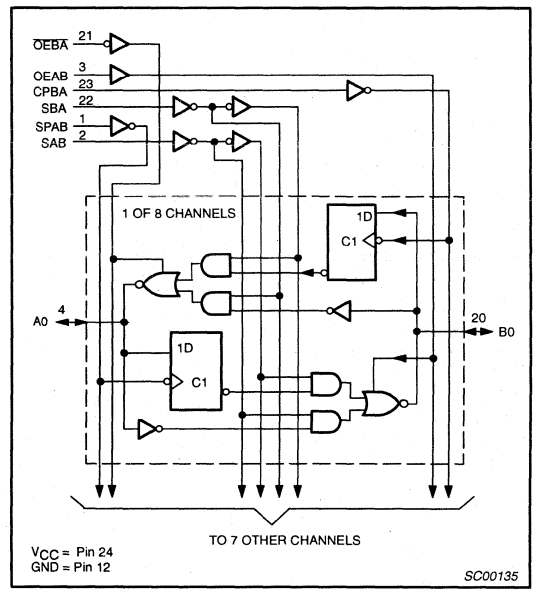
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALS651/74ALS651-1 and 74ALS652/74ALS652-1. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.



LOGIC DIAGRAM – 74ALS651/651-1



LOGIC DIAGRAM – 74ALS652/652-1



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	74ALS651/74ALS651-1	74ALS652/74ALS652-1
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, hold B	Store A, hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	S	Unspecified*	Input	Hold A, store B	Hold A, store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{B}$ data to A bus	Stored B data to A bus

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48 [1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
					I_{OH} = –3mA	2.4	3.2		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
		-1 versions		V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	control inputs		V_{CC} = MAX, V_I = 7.0V				0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V				–0.1	mA
I_O	Output current[4]			V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	74ALS651/ 74ALS651-1	I_{CCH}	V_{CC} = MAX			32	50	mA
			I_{CCL}				45	68	mA
			I_{CCZ}				44	68	mA
		74ALS652/ 74ALS652-1	I_{CCH}	V_{CC} = MAX			36	58	mA
			I_{CCL}				53	78	mA
			I_{CCZ}				49	72	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS FOR 74ALS651/74ALS651-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	LIMITS MAX	UNIT
f_{max}	Maximum clock frequency	Waveform 1	100		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	Waveform 1	5.0 6.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2, 3	1.0 2.0	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B Low)	Waveform 2, 3	6.0 5.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B High)	Waveform 2, 3	4.0 5.0	11.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	Waveform 7 Waveform 8	2.0 5.0	8.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	Waveform 7 Waveform 8	2.0 3.0	8.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 7 Waveform 8	2.0 5.0	9.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 7 Waveform 8	3.0 5.0	11.0 13.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74ALS652/74ALS652-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	Waveform 1	5.0 6.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2, 3	2.0 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B Low)	Waveform 2, 3	4.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn (A or B High)	Waveform 2, 3	6.0 5.0	14.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	Waveform 7 Waveform 8	2.0 5.0	8.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	Waveform 7 Waveform 8	2.0 3.0	8.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 7 Waveform 8	2.0 5.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 7 Waveform 8	3.0 5.0	11.0 13.0	ns

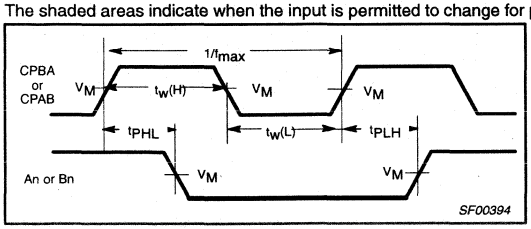
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, High or Low An or Bn to CPAB or CPBA	Waveform 4	5.0 5.0		ns
t_h (H) t_h (L)	Hold time, High or Low An or Bn to CPAB or CPBA	Waveform 4	0.0 1.0		ns
t_{su} (H) t_{su} (L)	Setup time, High or Low[1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0		ns
t_h (H) t_h (L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0.0 0.0		ns
t_w (H) t_w (L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	6.0 4.0		ns

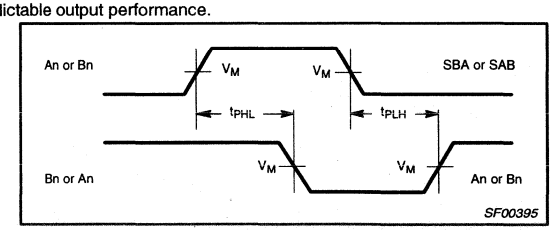
NOTE:
1. Setup time is to protect against current surge caused by enabling 16 outputs (24mA per output) simultaneously.

AC WAVEFORMS

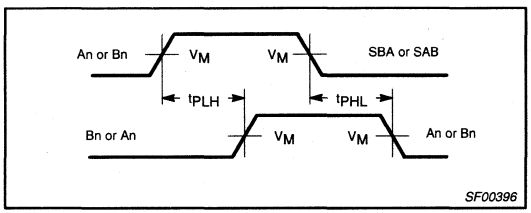
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



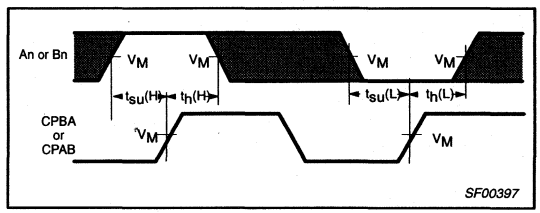
Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



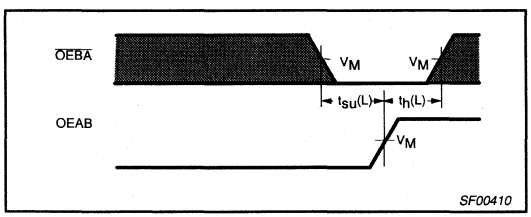
Waveform 2. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn



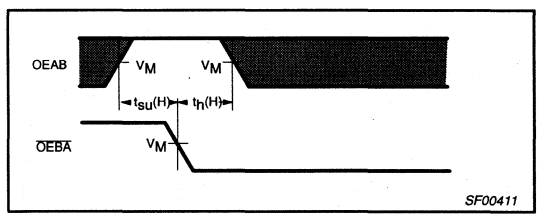
Waveform 3. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn



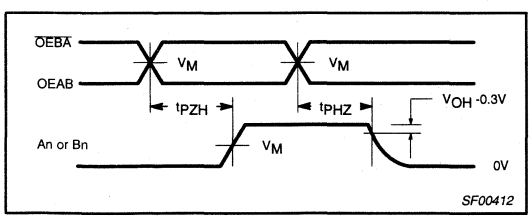
Waveform 4. Data Setup Time and Hold Times



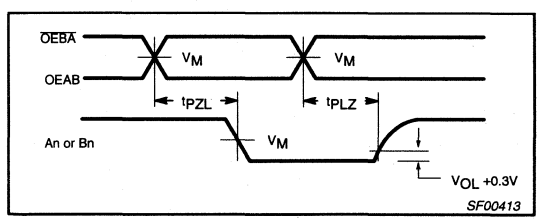
Waveform 5. $\overline{OEBA}$ to OEAB Setup Time and Hold Times



Waveform 6. OEAB to $\overline{OEBA}$ Setup Time and Hold Times

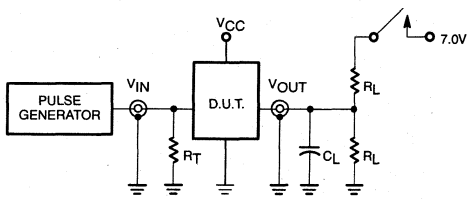


Waveform 7. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 8. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State and Open Collector Outputs

SWITCH POSITION

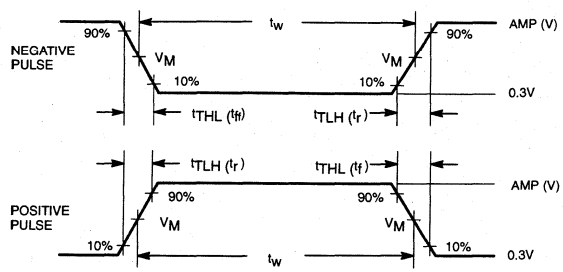
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
open collector	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00126

Section 3
Package Information

Advanced Low-power Schottky Devices (ALS)

CONTENTS

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when though-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"*.

THROUGH-HOLE MOUNTED PACKAGES

Table 1. Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24V) to the lead(s) of the package, below the seating plane or not more than 2mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2. Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapor phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Manual"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Table 3. Suitability of surface mounted packages for various soldering methods

Rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at and angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4mm**, e.g., SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

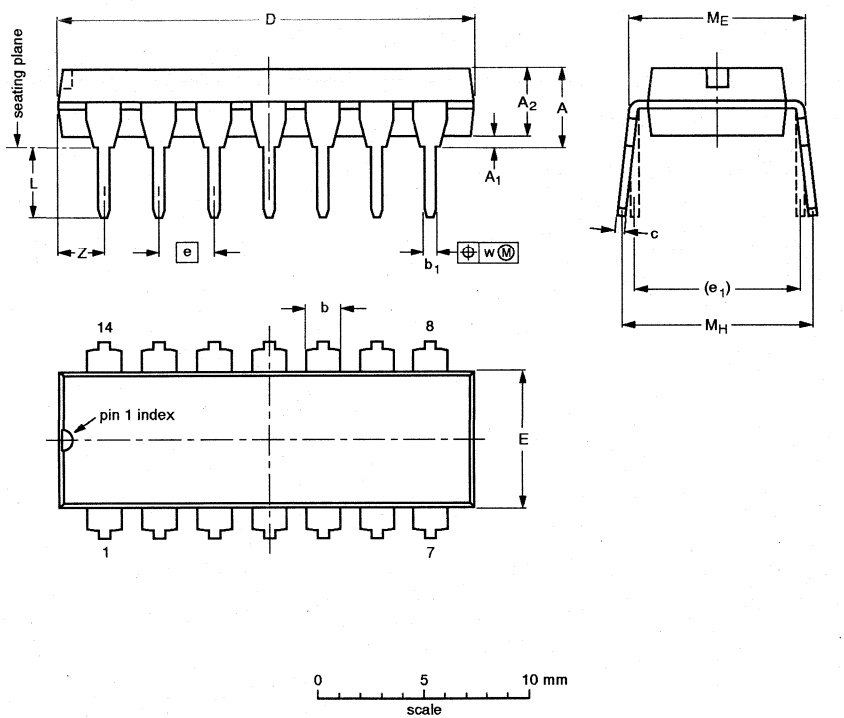
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C.

Package outline drawings for the ALS supplement

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

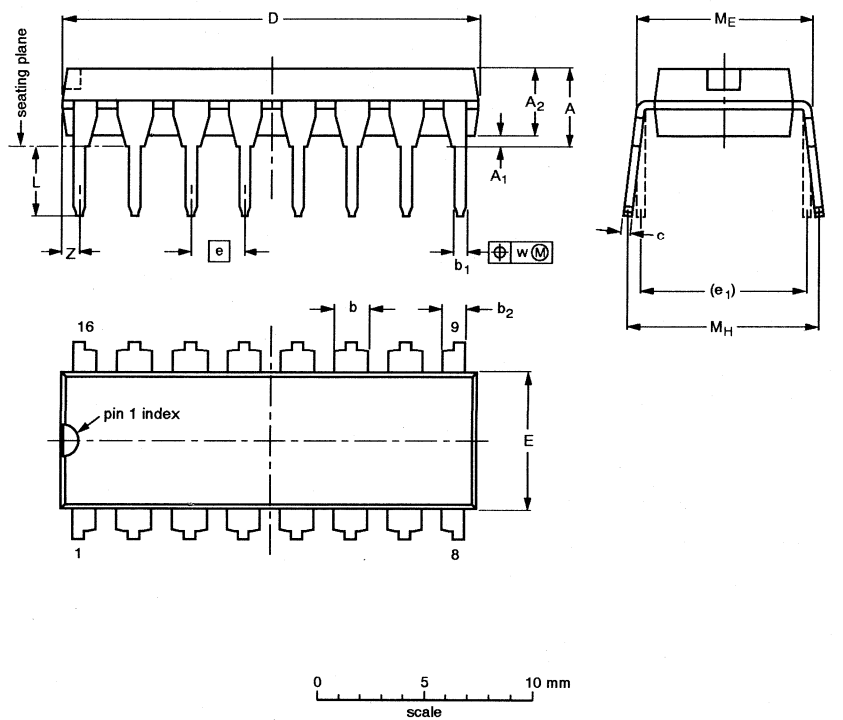
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Package outline drawings for the ALS supplement

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

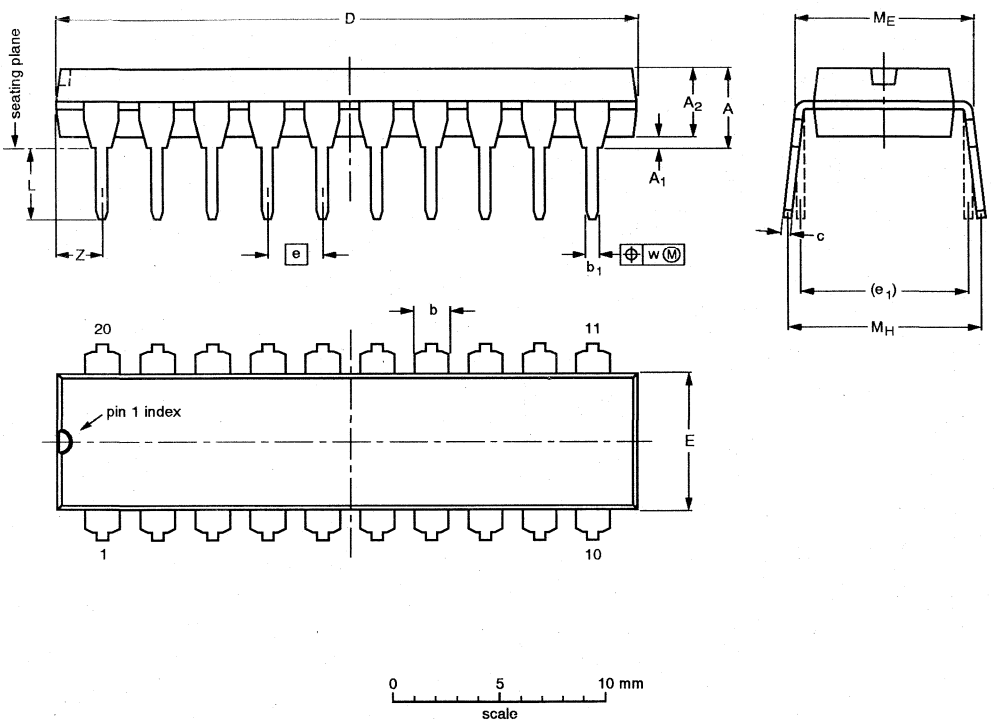
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Package outline drawings for the ALS supplement

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

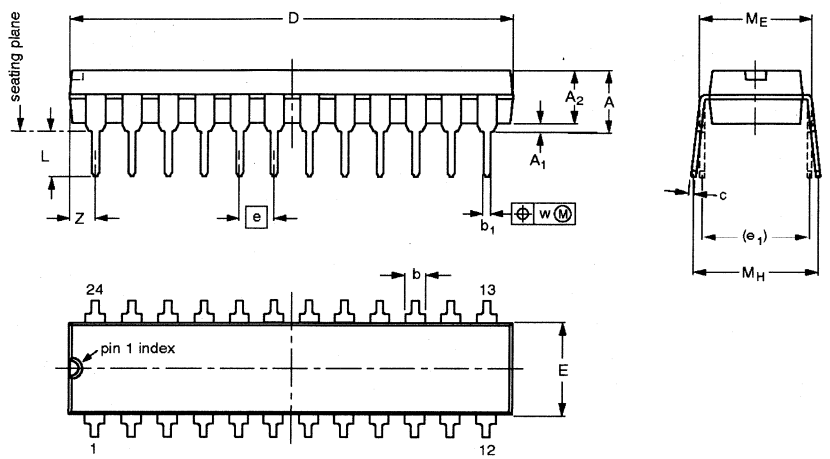
Note

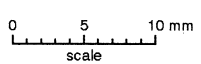
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Package outline drawings for the ALS supplement

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

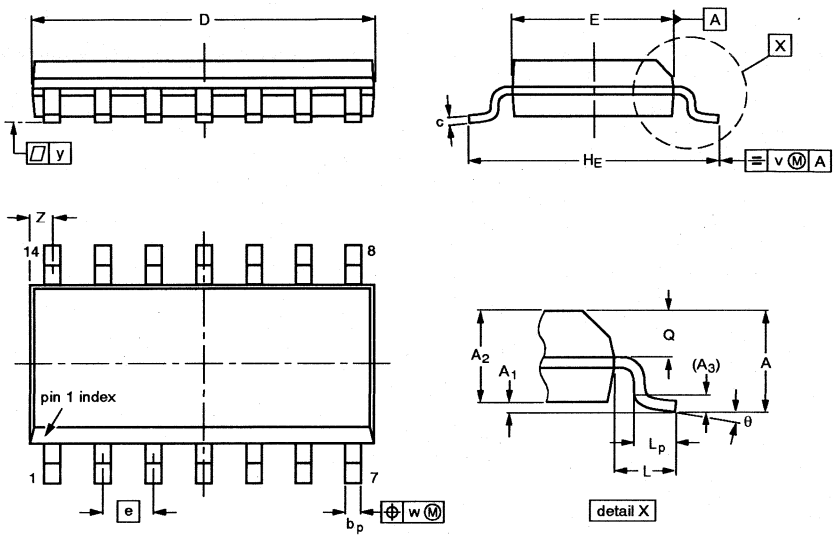
Note

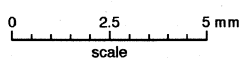
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Package outline drawings for the ALS supplement

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

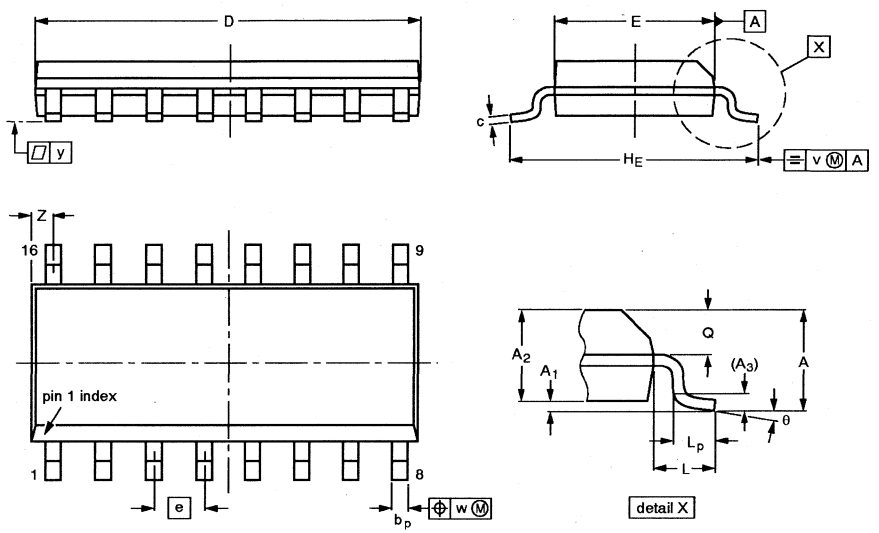
Note

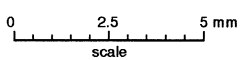
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

Package outline drawings for the ALS supplement

SO16: plastic small outline package; 16 leads; body width 3.9 mm — SOT109-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

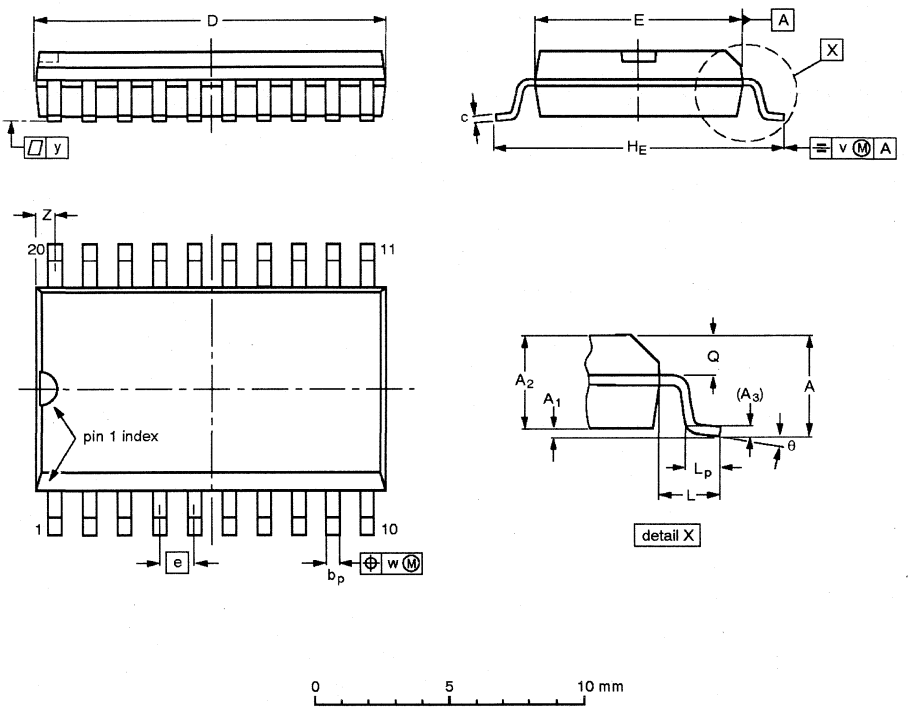
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

Package outline drawings for the ALS supplement

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

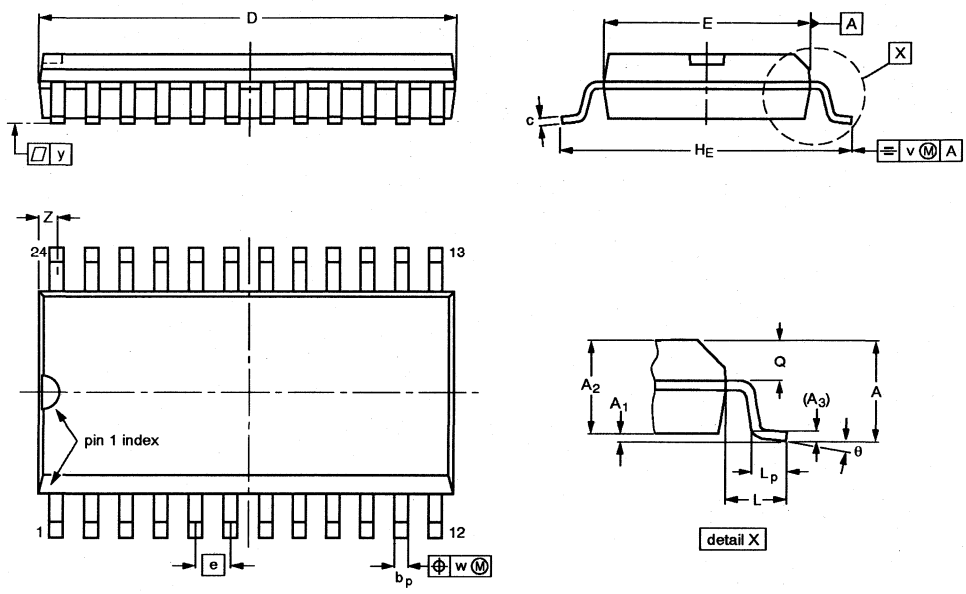
Note

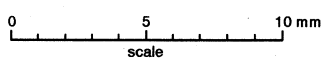
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

Package outline drawings for the ALS supplement

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

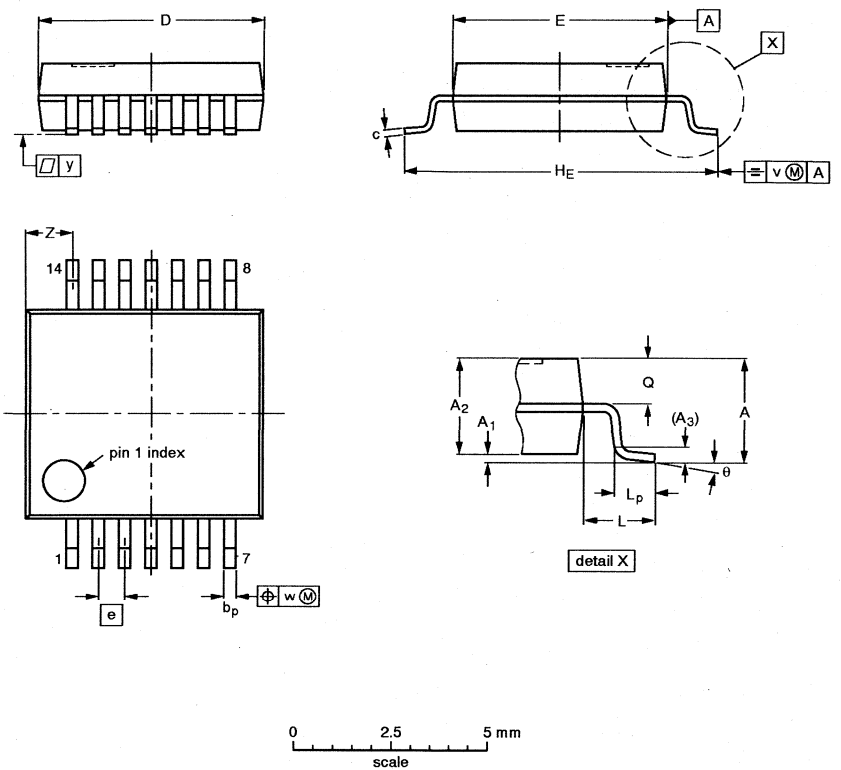
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

Package outline drawings for the ALS supplement

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm — SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

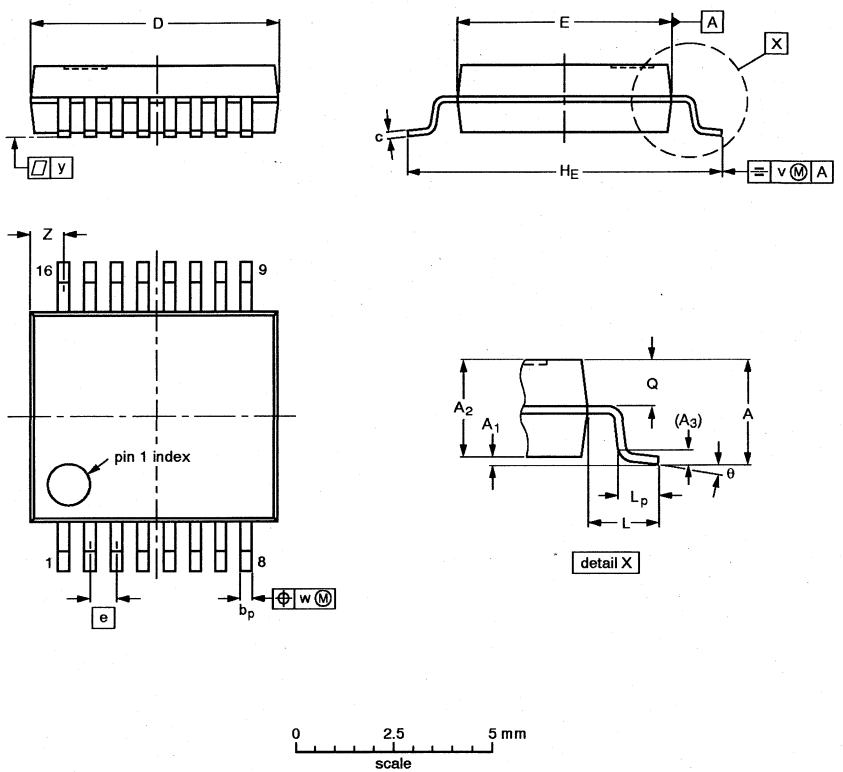
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

Package outline drawings for the ALS supplement

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm — SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

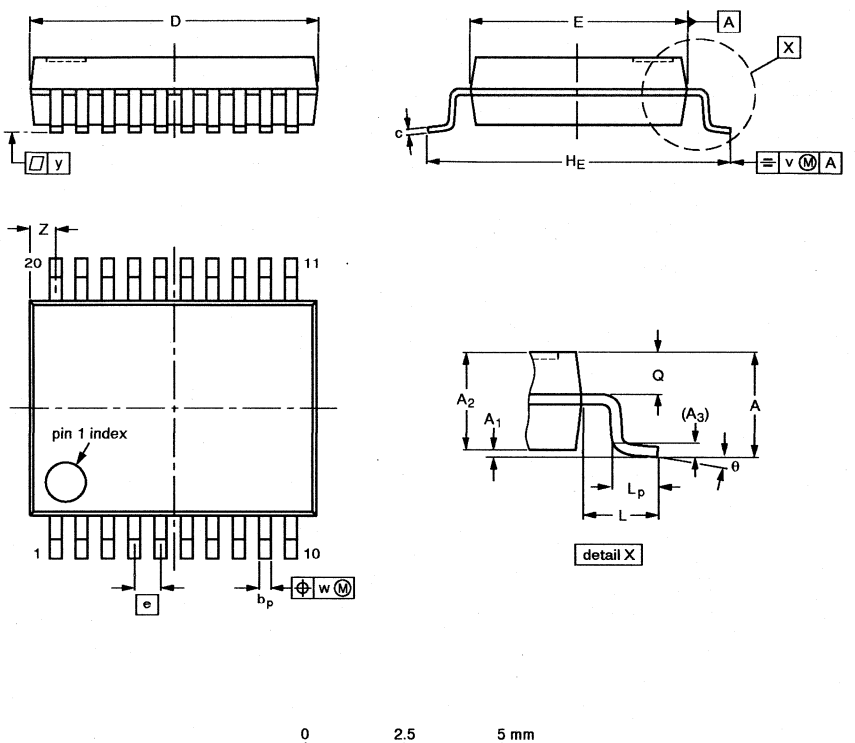
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

Package outline drawings for the ALS supplement

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm — SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

Data handbook system

Appendix A

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Wired Telecom Systems
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	I^2C Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	CMOS ICs for Clocks and Watches
IC17	Semiconductors for Wireless Communications
IC18	Semiconductors for In-Car Electronics
IC19	ICs for Data Communications
IC20	80C51-based 8-bit Microcontrollers
IC22	Desktop Video
IC23	BiCMOS Bus Interface Logic
IC24	Low Voltage CMOS & BiCMOS Logic
IC25	16-bit 80C51XA Microcontrollers (eXtended Architecture)
IC26	IC Package Databook

Discrete Semiconductors

Book	*Title*
SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Video Transistors and Modules for Monitors
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Transistors for HF and VHF
SC08b	RF Power Transistors for UHF
SC09	RF Power Modules
SC13	Power MOS Transistors including TOPFETs and IGBTs
SC14	RF Wideband Transistors
SC15	Microwave Transistors (new version planned)
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional Components

PC06	Circulators and Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?
For more information about Philips Semiconductors data handbooks, catalogs and subscriptions, contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook.** Product specialists are at your service and inquiries are answered promptly.

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display Components

Book	*Title*
DC01	Colour TV Picture Tubes and Assemblies Colour Monitor Tubes
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional Components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC12	Electron Multipliers

MORE INFORMATION FROM PHILIPS COMPONENTS?

For more information contact your nearest Philips Components national organizaiton shown in the following list.

Argentina: BUENOS AIRES, Tel. (541)786 7635, Fax . (541)786 9367.
Australia: NORTH RYDE, Tel. (02)9805 4455, Fax. (02)9805 4466.
Austria: WIEN, Tel. (01)60101 1820, Fax. (01)601 01 12 12.
Belgium: NL EINDHOVEN, Tel. (31)40 2783 749, Fax. (31)40 2788 399.
Brazil: SÃO PAULO, Tel. (011)821 2333, Fax (011)829 1849.
Canada: SCARBOROUGH, Tel. (0416)292 5161, Fax. (0416)754 6248.
Chile: SANTIAGO, Tel. (02)77 38 16, Fax. (02)735 3594.
China (Peoples Republic of): SHANGHAI, Tel. (21)326 4141, Fax. (21)320 2160.
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